Technologies Supporting Data Plane Control for a Carbon-Neutral Society

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Abstract

Data plane traffic in 5G mobile networks is expected to continue to grow rapidly in the future. Mobile communications providers face challenges in terms of location and power usage as they need to expand their facilities to accommodate this traffic. NEC is contributing to solutions by applying a variety of technologies to mobile networks. To preserve the global environment and pass it on to future generations, NEC is continually promoting R&D into carbon-neutral technologies and contributing to their implementation in society. This paper introduces some of the main technologies in this field.

Keywords

Carbon neutral, data plane, reduced equipment and facilities, reduced power consumption

1. Introduction

Data plane traffic in 5G mobile networks is expected to continue to increase rapidly in the future due to diversified use cases and richer content. Mobile communications providers are required to implement mobile networks compatible with large-capacity data traffic.

Meanwhile, mobile communications providers are also setting environmental goals for their business activities as activities to realize a carbon-neutral society gain momentum around the world.

Against this social backdrop, mobile communications providers are required to deal with continually growing traffic and to contribute to the implementation of a carbon-neutral society through a reduction of facilities and equipment as well as a reduction of power consumption.

This paper describes the technologies used to achieve these requirements.

2. Software Requirements for Data Plane Equipment

In the past, data plane devices in mobile networks were generally implemented as dedicated equipment that integrated software and hardware, but recent advancements in virtualization technology and software openness are enabling data plane devices to be implemented as a kind of software. As a result, it has become possible to create inexpensive, high-performance data plane devices using general-purpose hardware. On the other hand, for general-purpose equipment, a general-purpose operating system (OS) and general-purpose communication drivers are usually used. While these are easy to procure and have excellent cost performance and interoperability with various applications, they also have challenges such as operations using the general-purpose OS, inefficient hardware resource usage, and the need for highly difficult tuning to achieve power efficiency. The solutions to these challenges have become urgent tasks.

As a result of this technological evolution and current trends, the requirements for data plane equipment have changed from dedicated hardware to general-purpose hardware, from cloud native to high capacity, as well as carbon neutral.

2.1 Implementation of high-performance data plane software

NEC's data plane software achieves high performance without the need for tuning each server by maximizing the efficiency of hardware resource usage while understanding the characteristics of each type of hardware technology that is used. Low costs and high throughput are attained thanks to the diversity of general-purpose server choices. Specifically, NEC has established a method for data plane packet processing that aims to maximize the processing efficiency by using a general-purpose OS to achieve openness and by understanding the characteristics of CPU architecture, network devices such as the DPDK (Data Plane Development Kit), and functions provided by the general-purpose OS. We have established a method for data plane packet processing to maximize the processing efficiency (**Fig. 1**). Specific technologies for these aforementioned measures will be discussed in the following subsections.

2.1.1 Architectural transformation

(1) Simplified, more efficient processing
- **Faster memory access**
  With the CPU, every CPU core has a cache memory[*1] that serves a temporary storage of accessed data. To speed up the processing of an application, the cache hit rate (probability that the referenced data exists in the cache) can be increased to decrease the number of times that the physical memory is accessed. Because the size of the cache memory is very small, the data referenced

by the application is designed with the cache size in mind. Cache prefetching before accessing the data is considered as a way to improve efficiency. In addition, every CPU core has a cache called the translation look aside buffer (TLB) that stores the mapping between virtual and physical addresses. If access exceeds the cacheable limit, a TLB miss occurs and the memory access performance decreases. To prevent a TLB miss from occurring, data design is done so that the memory area referenced by the application running on the CPU core fits in the cache.

- **Faster execution of instructions**
  The CPU has a mechanism similar to a data cache that caches instructions. When the same processing is performed several times, access to the physical memory occurs the first time, but from the second time onwards, the instructions in the cache can be loaded and processed to thereby reduce the CPU load. To increase the efficiency of instruction cache usage, multiple packets are processed together (by bulking).

(2) More efficient CPU usage
- **Maximizing CPU usage efficiency**
  The CPU mounted in universal hardware has a multicore configuration. To maximize the efficiency of CPU resource usage without being affected by the number of CPU cores, processing independence is increased for each CPU core in conjunction with the aforementioned simplified software processing. Also, the system is designed so that the need for exclusive control between CPU cores is eliminated. Specifically, each CPU core is allocated an independent memory area and each user is assigned to a specific CPU core for processing. The number of CPU cores assigned for packet processing can be varied to maximize the performance per CPU core regardless of increases or decreases in the number of CPU cores.

2.2 Power savings

In general, the performance of an application is improved by adding advanced application processing. This results in an increase in CPU processing and tends to increase power consumption.

To achieve both high performance and power savings, NEC is promoting the following technological research (**Fig. 2**).
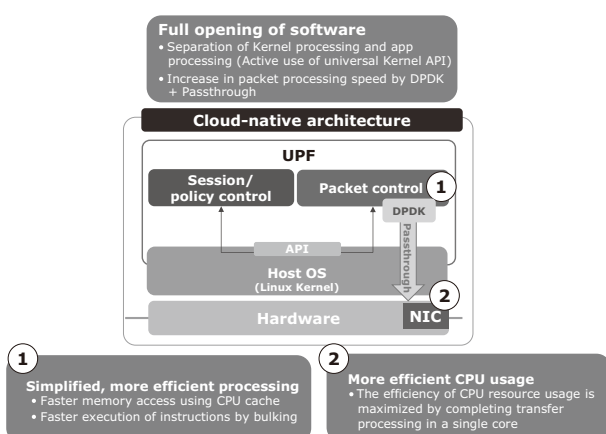

Fig. 1 Implementation of high-performance data plane software.

[*1] High-speed, small-capacity memory used by the CPU to retrieve or update information including data and instructions.
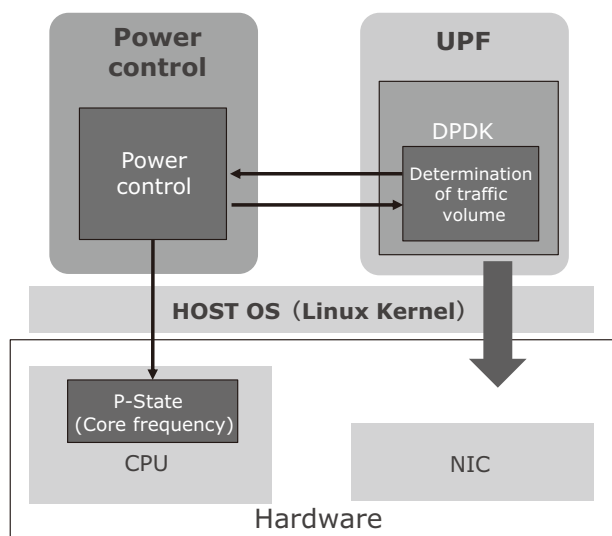
Fig. 2 How to attain power savings.

2.2.1 Processing offload to NIC

By replacing (offloading) some of the application functions with those provided by the network interface card (NIC) and by optimizing the software processing, the amount of CPU processing and the power consumption are reduced. Also, by minimizing the number of conditional branches in software processing, the entire process is simplified to achieve an even more efficient processing.

2.2.2 Power control technology

When processing packets using the DPUK, to achieve high performance, polling monitoring of the NIC is constantly performed, so the usage rate of the CPU core is always 100%. Usually, mobile communications providers design their facilities for peak periods, which are several hours a day. As a result, the operation rate is low most of the day, consuming more power than necessary. To solve this challenge, NEC is working on verifying the power optimization of server control in accordance with traffic volumes.

The power optimization of server control optimization enables a significant reduction of the power consumption in off-hours by dynamically controlling and optimizing the server CPU status in accordance with the volume of traffic.

3. Conclusion

As we move toward the Beyond 5G/6G era, general-purpose technologies such as the CPU and the NIC will also evolve. We believe that one day we will live in a world where heterogeneous computing[*2] is realized by combining the advantages of each and every vendor.

NEC continues to contribute to the advancement of mobile networks and the resolution of social issues by quickly adopting cutting-edge technologies that take advantage of the characteristics of general-purpose hardware.

4. Acknowledgements

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*2 Computer system built by combining different types of processors.

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