Variation-Aware Design for Nanometer Generation LSI

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Abstract

Advancement in the microfabrication of semiconductor chips has made the variations and layout-dependent fluctuations of transistor characteristics noticeable. It is necessary to develop a design technique that can predict the above phenomena and their effects from the design stage, in order to exploit the maximum performance of transistors and implement high-performance LSIs at low costs. This paper is intended to introduce the efforts made by NEC Electronics for designs considering variations and layout dependence.

Keywords

semiconductor, variation, Monte Carlo simulation, layout, transistor, interconnect, microfabrication

1. Introduction

Advancement in the microfabrication of transistors and interconnects has led to an increase in the variations of device
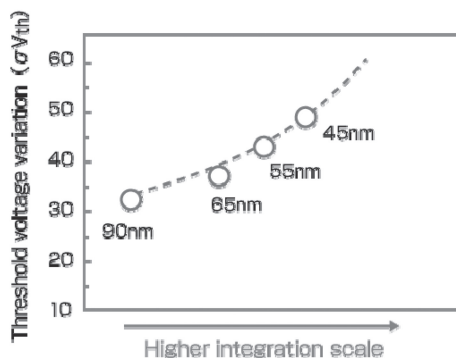

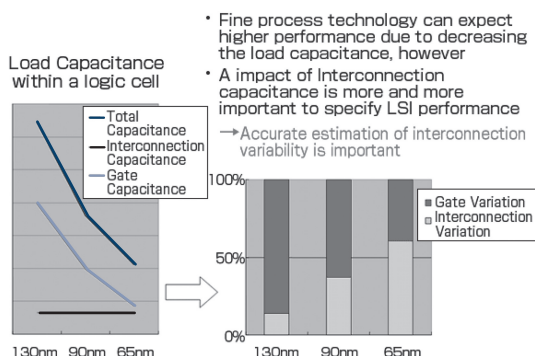Fig. 1   Variation in threshold voltage between process generations.

Fig. 2   Impacts of interconnect variation.

characteristics. As shown in **Fig. 1** , variations in threshold voltage for turning the transistor on are increasing following the advance of microfabrication. Also, **Fig. 2** shows that the share of interconnect capacitance in the load capacitance of LSI logic cells, such as inverters and NAND, etc., and the effects of variation among interconnects are also getting higher than before. Therefore, the design of LSIs for the nanometer generation (here, we will call processes of 90nm and below "nanometer generation" processes) requires consideration of the variations among interconnects as well as those among transistors.

In this paper, we will introduce our efforts for variation-aware design, which is the foundation supporting the transistor-level designs of LSI components, such as logic cells, SRAM macros, analog macros and high-speed interface macros.

2. Visualization of Variations and Its Application to LSI Design

To design an LSI by considering variation, it is critical to break down variations according to the factors causing them, and then model these factors.

As shown in **Fig. 3** , variations among transistors can be classified roughly as "die-to-die variation" and "within-die variation."

The effects of "die-to-die variation" are observed in the differences between chips in the delays in internal clocks and signals. The effects of "within-die variation" are observed in the timing error between clocks and signals and in the offset of opamps.

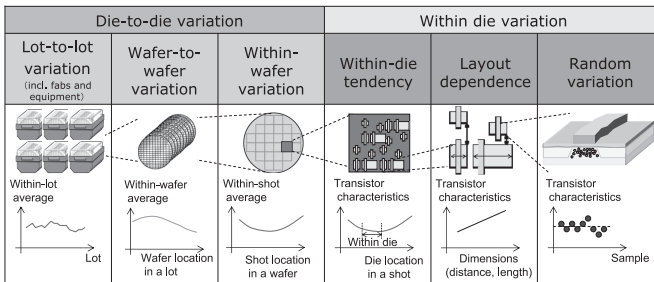The "die-to-die variation" has been dominant up to around

Fig. 3   Breakdown of transistor variations by factor.

Table   Variation factors and corresponding design techniques.
Blue characters：Technology applied for the nanometer generation

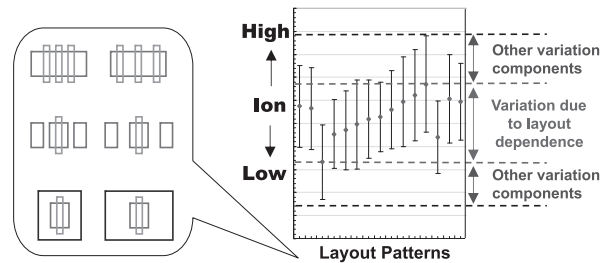| Item	Die-to-die variation	Within-die variation	
		Layout dependence	Random variation
Transistor	•SPCE corner model	•Layout-aware LPE	•Monte Carlo simulation（Statistical SPICE model）•Pelgrom plot
Interconnect	•Corner LPE（Statistical variation-aware）	•Layout-aware interconnect model	—

Fig. 4   Variation of saturation current (Ion) due to layout dependence.
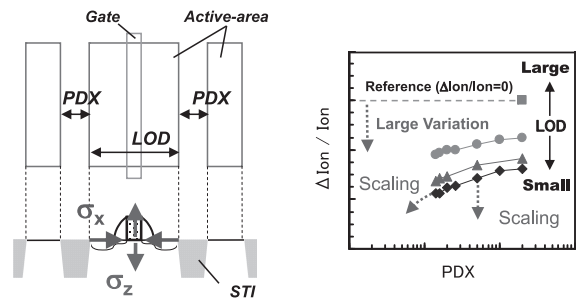
Fig. 5   Variation of saturation current (Ion) due to STI stress.

the 130nm generation. As a result, LSI design has been possible using relatively simple models that directly add the "within-in-die variation" to the "die-to-die variation" such as the fast corner model, which assumes the case in which all transistors can be high-speed transistors, and the slow corner model, which assumes the case in which all transistors can be low-speed transistors.

As the nanometer generation has come, and the microfabrication of transistors has advanced, the share of "within-die variation" has increased, making it necessary to use new models to represent the "within-die variation" that has not been able to be considered with the previous models, and to develop corresponding design techniques ("variation-aware design").

Table classifies the variation-aware designs and layout-aware designs we adopted for the nanometer generation according to the factors causing variations. In Section 3 and after, we will introduce each of the design techniques we adopted for the nanometer generation, shown in blue characters in Table.

3. Layout–Aware Design

3.1 Layout–Aware Design of Transistors

Microfabrication of transistors has made noticeable their layout dependence, with which transistor characteristics vary even when gate length (L) and gate width (W) are identical, depending on the shape of areas other than channel areas and on the distance from adjacent transistors.

Fig. 4 shows an example of saturation current (Ion) variation depending on layout, obtained by using transistors of identical L and W and changing the surrounding layout in many ways. Each plotted point represents the pure layout dependence after the other variation components are eliminated, and each error bar is the variation width of measurement data and represents the variation component other than that dependent on the layout. This example shows that more than half the variations of transistor characteristics are layout-dependent.

Fig. 5 shows an example of Ion variations when the length of the active-area (LOD) or the distance from the adjacent active-area (PDX) are changed. These variations are caused because the stress (lattice strain) due to the difference in thermal expansion coefficient between the silicon of the active-area and the silicon oxide in shallow trench isolation (STI) varies depending on the amplitudes of LOD and PDX. As microfabrication has led to a decrease in the minimum sizes of LOD and PDX, this characteristic variation has become more noticeable than before.

At NEC Electronics, we built an environment for

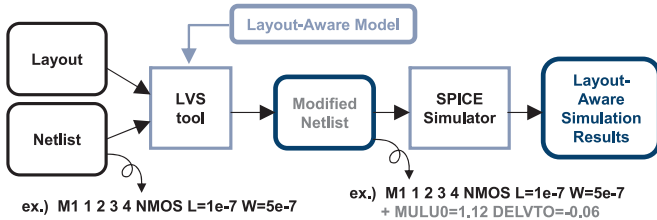Fig. 6   Flow of layout-aware design.

Fig. 7   Layout dependence of interconnect cross-section shape.

reproducing the characteristic variation caused by layout dependence by means of simulations, without adding any process to the traditional design flow. **Fig. 6** shows the design flow. This flow (1) reads the geometrical information related to the characteristic variations (which correspond to the LOD and PDX described above) from the layout data at the time of layout-versus-schematic (LVS) collation, conducted after the layout design; (2) calculates the amounts of variations in transistor characteristics using layout-dependent variation models; and (3) outputs a SPICE netlist reflecting the calculation results. In the SPICE netlist, the amounts of characteristic variations are specified with MULU0, DELVTO, etc. The variations can be reproduced by performing a SPICE simulation using the SPICE netlist.

The models of layout-dependent characteristic variations include a model originally developed by us, the model developed in MIRAI-Selete [1] and the characteristic variation model incorporated in the SPICE model.

As this method eliminates the need to incorporate the variation in transistor characteristics due to layout dependence in the design margin, the guard-band width can be reduced by half and the LSI performance improved by up to about 20%.

3.2 Layout−Aware Design of Interconnects

Microfabrication of interconnects has also made the layout-dependent variation in the cross-sectional shape of interconnects noticeable. As shown in the left diagram in **Fig. 7** , the upper surface of the large-width interconnect is scraped excessively (dishing) with CMP (Chemical Mechanical Polishing), and the sides of interconnect are not always processed vertically. The thickness of the barrier metal film formed between the interconnect material and the insulation film is also dependent on the interconnect width. The right diagram in Fig. 7 shows the variation of cross-sectional shape caused by the changes in interconnect density. It shows that, in the high-density domain, interconnects are scraped excessively (erosion) with CMP together with the insulation films in the
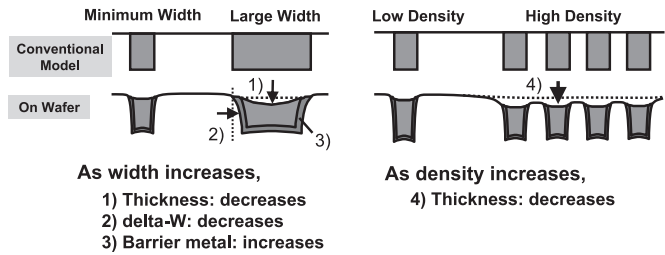
surroundings.

These variations in the cross-sectional shape cause the variations of the parasitic resistance and capacitance of interconnects. As microfabrication has advanced, and the sizes of interconnects have consequently reduced, the effects of variations in shape have become larger than before. As a result, a significant error will occur if the traditional interconnect model, composed of a simple rectangle that assumes that the interconnect width according to the layout size and the interconnect film thickness according to the target thickness are possible, is applied in fine interconnects.

At NEC Electronics, we developed an interconnect model that can reproduce the layout dependence of interconnects [2] , and applies it to the LPE (Layout Parameter Extraction), in which the parasitic resistance and capacitance of interconnects are extracted, to reduce the above-mentioned error. While the previous technique used to produce an error of up to around 10% in the interconnect delay, due to the errors in parasitic resistance and capacitance due to the cross-sectional shape, the new technique, reproducing layout dependence, can minimize these errors.

Introduction of this technique eliminates the need to incorporate the variation in interconnect characteristics due to layout dependence in the design margin, and reduces the guard-band width, thereby achieving an ease of design and improvement of performance.

4. Within−Die Variation−Aware Design of Transistors

The threshold voltage and drain current of the transistor vary randomly due to random fluctuation of the impurities implanted below the gate to control the threshold voltage, and to those of the gate length due to exposure or etching. The effects of random transistor variations can be predicted using statistical techniques such as the Monte Carlo simulation. Some of commercially available SPICE simulators incorporate the
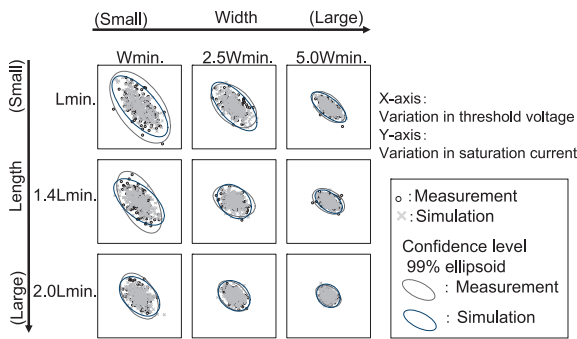
Fig. 8   Comparison of model and actual data using the principal component analysis technique.

function for executing the Monte Carlo simulation by combining it with SPICE models describing parameters representing variation (statistical SPICE models).

A technique has been developed that makes use of principal component analysis for implementing statistical SPICE models reproducing the correlations of several variations, such as those of threshold voltage and drain current [3] . The use of the principal component analysis technique makes it possible to realize statistical SPICE models capable of reproducing transistor variations with a small number of parameters.

Fig. 8 shows the actual data on the variations of threshold voltage and saturation current of transistors with various gate lengths (L) and gate widths (W), and the simulation results using the statistical SPICE models developed with the principal component analysis technique. It shows that these statistical SPICE models are capable of reproducing the correlation between variations and the dependences of L and W very well.

At NEC Electronics, we have developed statistical SPICE models capable of reproducing random transistor variations accurately, and utilizing them in prediction of the effects of variations.

5. Die–to–Die Variation–Aware Design of Interconnects (Corner LPE)

Increasing variations among transistors and interconnects have been deteriorating the closure of clock and signal timing verifications, and this has made it important to optimize the variation width that is set as a corner condition in timing verifications. This section describes a technique for optimizing the variation of interconnect delay to be used in timing verifications.
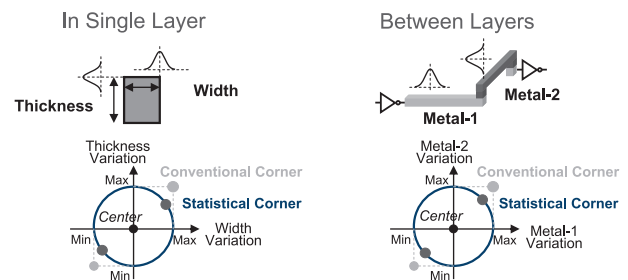

Fig. 9   Interconnect variations and corner condition setting technique.

The left diagram in **Fig. 9** shows the relationship between variations of the width and film thickness of interconnects formed on the same interconnect layer. Since the width and film thickness of interconnects are determined by different processes, they vary independently of each other. The conventional technique set the shape in which variations in width and film thickness are respectively maximum and minimum as corner conditions. As a result, the cross-sectional shape under corner conditions would become the one whose existence is statistically impossible, so the interconnect delay under corner conditions should contain an excessive amount of margin. The same also applied to the variation of interconnects formed on different interconnect layers, as shown in the right diagram of Fig. 9.

At NEC Electronics, we developed a technique for the statistical setting of the corner conditions that can maximize or minimize the signal delay so as to achieve an optimum variation [4] , and applied it to the design (statistical corner conditions shown in Fig 9).

As a result, we succeeded in reducing the guard-band width from the fast corner to the slow corner by about half compared to the conventional corner conditions. This also led to an improvement of LSI performance by up to about 15%, as well as an improvement in ease of design and reductions in chip size and power consumption.

6. Conclusion

As discussed above, we have developed design techniques featuring optimum prediction of transistor and interconnect variations, by developing physical models for reproducing these variations and layout dependences and applying these models to actual design. In the future, we will continue modeling variations caused by new physical phenomena accompa-

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nying microfabrication, and promote the development of low-cost, high-performance LSIs.

References

1) K. Yamada et al.; "Layout-aware compact model of MOSFET characteristics variations induced by STI stress", IEICE Transaction on Electronics, vol.91, no.7, pp.1142-1150, 2008

2) K. Yamada et al.; "Accurate Modeling Method for Deep Sub-Micron Cu Interconnect", VLSI Symposium on Technology, pp.111-112, 2003

3) K. Takeuchi et al.; "A Highly Efficient Statistical Compact Model Parameter Extraction Scheme", SISPAD 2005 Proceedings, pp.135-138, 2005

4) K. Yamada et al.; "Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)", Asia and South Pacific Conference on Design Automation, pp.706-711, 2006

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