R&D of LSIs Aiming at High Reliability, High Performance and Low Power Consumption

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Abstract

The LSI Fundamental Research Laboratory, NEC Electronics, is developing materials, processes, devices and circuits required for the establishment of high reliability, high performance, low-power consumption devices that can satisfy the needs of our customers. This paper is intended to introduce some of the recent research activities of the laboratory in the fields of the key CMOS basic-technologies (FEOL/BEOL) and of the performance-boosting technologies (RF/circuit/variation-control, etc.).

Keywords

variation control, MOSFET, multilayer interconnecting, high-speed interface, passive component

1. Research Strategy of the Laboratory

At the LSI Fundamental Research Laboratory, we promote the vision "to become the global leader in semiconductor research that can create technological innovations aimed at earning the confidence both of our customers and of society." To this end we set the "key CMOS technology" in pursuit of scaling-down and the "differentiation technology for boosting CMOS performances" as the two pillars of research for maintaining the distinctiveness of NEC Electronics and in order to provide it with keener competitiveness. We are enabled thus to implement LSIs that can be used with satisfaction by our customers.

The "key CMOS technology" consists of achieving increase in speed, reduction of power consumption, increase of density and reduction of costs of transistors mainly as a result of scaling. However, since the advancement of scaling necessitates large development-expense, we aim to promote efficient development in this field within the framework of global joint-research-systems. In the future, research will not remain merely in the field of scaling but will attempt to exceed its physical limits by introducing new materials and new device structures that are expected to increase in importance.

While the "key CMOS technology" is becoming more commonplace with the spread of global research systems, the "differentiation technology" research has been getting more important than ever because it allows each business to enhance the added values of their LSIs. At present, the research domains that our laboratory is tackling include; 1) variation control technology for scaled-down CMOS devices; 2) device simulation technology; 3) next-generation embedded memory technology (eDRAM, etc.); 4) low power, high reliability interconnect technology; 5) high speed I/O analog device technology; 6) low power circuit technology, etc. We are planning to make our products more attractive by making use of the results of the above research. Below we introduce some of the results of our device research (**Fig. 1**).

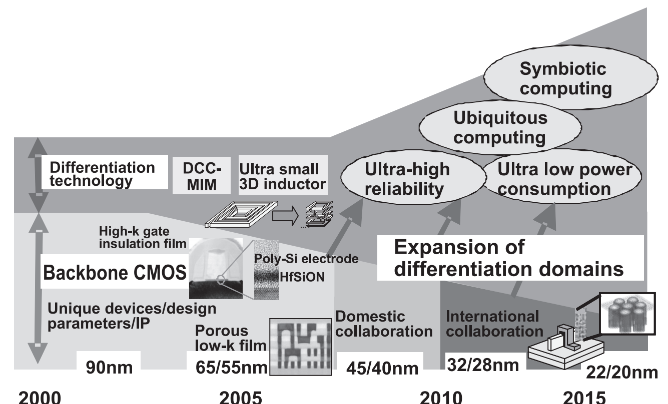

Fig. 1 Development of key CMOS technology and differentiation technology.

2. Transistor Variation Control Technology

With LSIs of the 90nm generation and after, the random variation of transistor characteristics has been increasing rapidly, thus making the countermeasures aimed at variations one of the critical differentiation domains determining the issues of

product development. Based on these circumstances, we are conducting research activities for enabling high reliability design procedures that incorporate a clear understanding of the physics of variation. Specifically, they include the fundamental technologies for variation evaluation such as a special TEG design for variation measuring followed by parameter extraction for statistic SPICE, activities for understanding the physics of variation through theories and TCAD, and the development of a statistical design technique for rational design that can deal efficiently with variation.

Here, we will describe the atomic-level TCAD simulation technology, which is a tool for understanding the physics of variation. Recent research including our own has clarified that fluctuations of the location and the number of impurity atoms introduced in the transistor are the main causes of the random variation of MOSFET. This technology simulates a lot of transistors in which the location and number of impurity-atoms are fluctuated by stochastic simulation on a computer, in order to visualize microscopic variation phenomena that are difficult to observe directly with the naked eye. A clearer understanding of the physical principles is thus facilitated.

For example, we discovered that, when a voltage is applied across the source and drain terminals of a transistor, an “abnormally distributed DIBL (Drain-Induced Barrier Lowering)” with which the threshold voltage varies in a distorted manner unlike the normal distribution. We found that this variation derived from the halo structure regarded as being indispensable in the nano-fabrication of transistors by using the simulation technology as shown in **Fig. 2** . We were thus able to draught the design guidelines for a transistor that is less affected by this phenomenon by adjusting the impurities concentration distribution in the halo structure.

In addition, we also established a circuit simulation technique enabling an accurate evaluation of the effects of variation on circuit characteristics and a design technique for implementing high-quality embedded-SRAM that is expected to be miniaturized further in the future. These innovations have made it possible for us to design high-quality SRAM with high yields.

3. Low Power Consumption CMOS Devices

The advancement of the nanofabrication of devices has made the issue of the significant increase in leak current more noticeable. Particularly, reduction of junction leak current is extremely important for the implementation of low-power embedded-DRAM. We are therefore promoting research into the structure and process technology of the transistor’s diffusion layer, aiming at performance improvements for most advanced LSIs as well as to significantly reduce the leak current (**Fig. 3**).

The newly developed solutions consist of the following three element technologies. The first is the implementation of the elevated diffusion layer structure, with which a Si (silicon) film with a facetted (tapered) surface is deposited on the shallow diffusion layer near the gate, called the extension, as well as in the deep diffusion layer, called the source/drain domain. As a result, the diffusion layer becomes a thick film and the parasitic resistance is reduced, so the ON current can be increased by about 60% and the increase in the parasitic capacitance between the gate and source/drain due to the formation of the facetted surface can be reduced, thereby reducing the operation power by about 30%. Next, we injected impurities into the deep diffusion layer called the source/drain domain, by

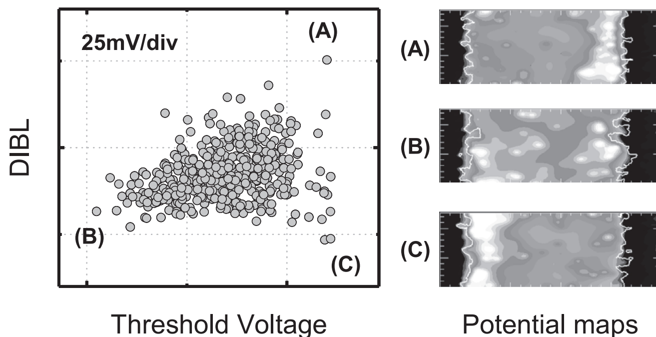

Fig. 2 Potential distribution in channel domain, obtained from abnormal DIBL distribution and TCAD simulation.

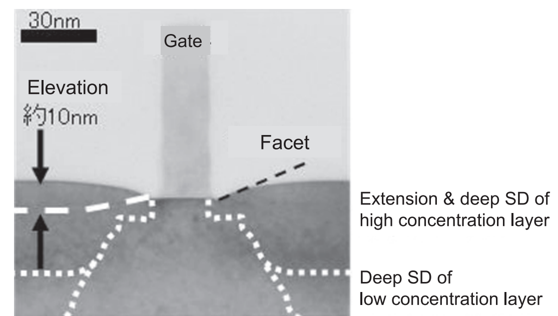

Fig. 3 High-performance MOSFET with elevated diffusion layer structure.

injecting high concentrations into the upper layer and low concentration into the lower layer. As a result of this procedure we succeeded in reducing the resistance at the boundary with the silicide in the upper layer. In the lower layer, we also succeeded in reduction both of crystalline defects and the junction electrical field to reduce the leak current. Additionally, we also adopted a new millisecond annealing technique, which is a thermal treatment method for activating the impurities injected into the diffusion layer by applying annealing at a relatively low temperature for a few seconds before and after the high-temperature millisecond annealing. As a result, we succeeded in improving the activation rate and the crystalline defects contained inside the diffusion layer by promoting the limited out-diffusion of impurities, thereby reducing the junction leak current to below 1/1,000th that of the previous technique.

The technology described above will also make it possible to increase the operation speed and decrease the power consumption of most advanced system LSIs such as the DRAM-embedded LSI (embedded DRAM, or eDRAM) that is subject to such severe requirements with regard to low-leak performance.

4. Low Power Multilayer Interconnect Technology

The recent miniaturization of processes has decreased the intervals between interconnects connecting transistors, and this has caused the problem of an increase in the operating power consumption of LSIs due to increases in the parasitic capacitance in the interconnects. As it is required to reduce the parasitic capacitance to reduce the power consumption, research on the porous Low-k film material is being actively conducted to reduce the relative permittivity (k) to below 2.5. This is being done by introducing pores into the insulation film and in particular by aiming at the LSIs of the 40nm generation and after (**Fig. 4**). However, it is also known that the introduction of pores in the inter-layer insulation layer causes certain problems, such as absorption of moisture or the introduction of processing damage during the LSI manufacturing process.

To deal with these problems, we developed a new vapor phase deposition process, which provides the precursor molecules with pores as the origin of the porous structure, and stacks the molecules by means of plasma reactions (**Fig. 5**).

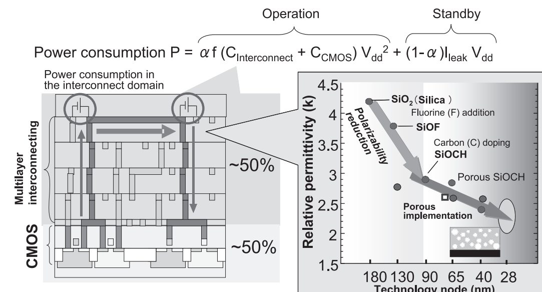

Fig. 4 Development trends of Low-k materials for LSI multilayer interconnect.

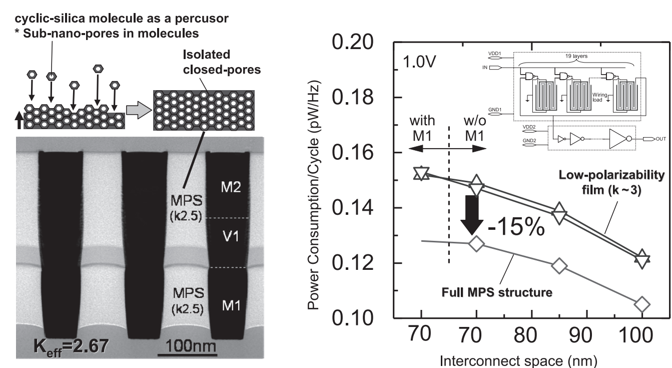

Fig. 5 Cross-sectional TEM micrograph of multilayer interconnect using MPS film, its LSI power consumption reduction effect.

Furthermore, we also developed a process and equipment for the film deposition that is compatible with 300 mm wafers through the MIRAI Project [*1] , and succeeded in obtaining a MPS (Molecular Pore-Stack) film material (k ~ 2.5) composed of isolated 0.4nm pores that does not allow water molecules to be diffused, achieving high reliability and low permittivity among scaled-down interconnects. We also developed a robust multilayer interconnect module that is composed of “full-MPS film with copper conductor.” When we verified it in the 40nm process, we confirmed that power consumption in the interconnect domain can be reduced by about 15% compared to the previous process using the low-polarizability film (k ~ 3).

Aiming at reduction in the operation power consumption of LSIs, we intend to enhance our research into the Low-k film material and interconnect modules with lower permittivity and higher reliability.

[*1] We participated in the MIRAI (Millennium Research for Advanced Information Technology) Project “Low-Permittivity Materials and Interconnect Module Technology” held between July 2001 and March 2004 (Phase 1) and between April 2004 and March 2006 (Phase 2), and developed the plasma copolymerization technology, 300mm MPS film deposition process and equipment technology. The research results of this project have already been transferred to us.

5. Ultrahigh-Reliability Interconnect Technology

Leading-edge LSIs, especially for automobile applications, require high reliability in their multilayer interconnect layers. Nevertheless, the advancement of miniaturization has brought about a significant increase in the resistance of Cu interconnect and has deteriorated its reliability noticeably. It is necessary to improve the crystalline properties of the Cu film of the interconnect in order to solve these technological issues thoroughly. Therefore, we developed a high-quality Cu multilayer interconnect by introducing the new “ruthenium (Ru) / titanium (Ti) stacked barrier structure” featuring excellent crystalline matching with the Cu film (**Fig. 6**).

The Ru/Ti stacked barrier film is grown using a low-cost conventional sputtering process. As a result, the Cu crystalline property in the interconnect has been improved thanks to the good crystal lattice matching with the Cu crystal stable plane (plane (111)) of Ru compared to the currently used Ta/TaN stacked barrier. Also, the via hole resistance has been reduced by 70% thanks to the low specific resistance of the Ru (~20mΩ・cm) compared to that of TaN (~240mΩ・cm).

Ti used as the under-layered film of the Ru film also plays an important role. In general, the Ru film itself does not have function as a barrier against Cu diffusion, but we discovered that it can be provided with a barrier function by diffusing Ti in the grain boundary of the Ru film. The Ti film is formed on the lower Cu interconnect at the bottom of the via holes, Ti is also diffused in the grain boundary of the lower Cu interconnect and can therefore restrict the diffusion of Cu atoms near the via holes. By improving the quality of the Cu crystals and partial doping of Ti to the via hole bottoms, we were able to suppress the electro-migration of Cu atoms in the proximity of the via holes and confirmed extension of the EM life by 35 times compared to that of the conventional Ta/TaN barrier structure.

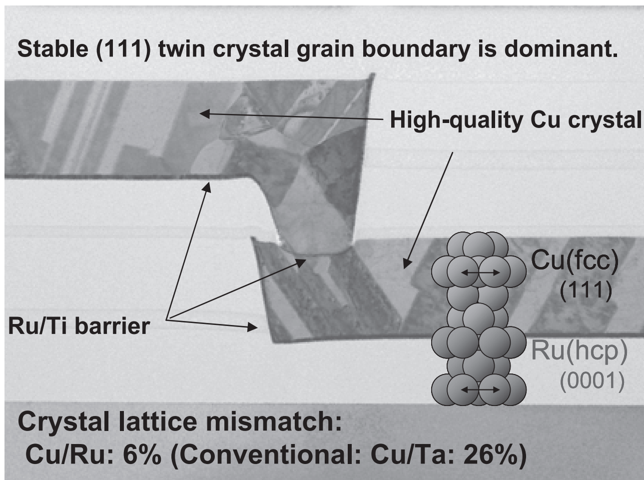

Fig. 6 High reliability Cu interconnect composed of high-quality Cu crystal using Ru/Ti barrier structure.

As a result, we confirmed the possibility of implementing a low resistance, ultrahigh-reliability Cu interconnect that is compatible with high temperatures operation above 150°C.

6. Ultracompact On-Chip Inductor with Low-Power I/O Compatibility

The high-speed digital LSI needs a high data processing speed of the Gbps class and achieves such high-speed operation using the CMOS current-mode logic (CML) circuit that performs signal shaping by using on-chip inductors as shown in **Fig. 7** . However, the previous inductor element has a large footprint due to the planar winding of the upper-layer interconnect with large interconnect widths, so its applications have been limited due to the increased cost that resulted from the increased chip area.

To deal with this problem, we adopted the fine-pitched Low-k/Cu multilayer interconnect located in the lower layers in the LSI and developed a “3D solenoid type on-chip inductor” composed of a spiral circle of inductor interconnect (**Fig. 8**).

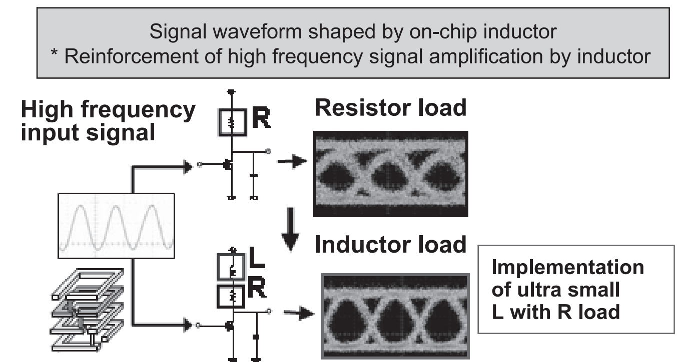

Fig. 7 CMOS current mode logic circuit using on-chip inductors.

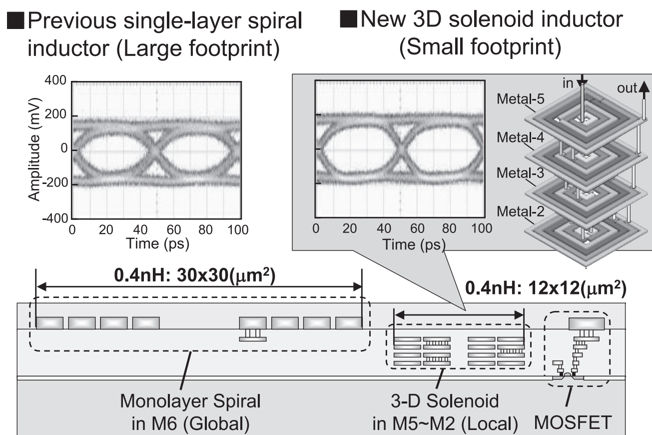

Fig. 8 Eye pattern used in application of 3D solenoid inductor in 20Gbps D-F/F circuit.

We verified that this structure could reduce the footprint to 1/6th while maintaining an equivalent high-speed response to the traditional planar on-chip inductor with a large footprint. We combined the new inductor element with the advanced CMOS CML circuit, verified the operation and confirmed a high-speed signal processing performance of 20Gbps at 1V voltage.

This 3D conductor element is a new means for promoting improvement in performance, cost and power consumption of the LSI in addition to the scaling of the CMOS device. When it is combined with the leading-edge CMOS device, it will be possible to improve the performance cost-effectively, and reduce the power consumption in ubiquitous equipments handling ultrahigh frequencies and high-speed signals such as high-speed, large capacity servers.

7. Conclusion

Our laboratory is developing the materials, processes, device structures and circuit technologies as well as the technology for their integration that is required to establish devices that feature high reliability, high performance, multiple functions and low power consumption. We will thus be able to implement higher performance LSI devices that can effectively satisfy the needs of our customers.

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