Development of Single-Frame Super-Resolution System LSI

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Abstract

NEC Electronics has developed a system LSI using the "single-frame super-resolution technology." This technology has been developed jointly with NEC Central Research Laboratories. This paper describes the IP (Intellectual Property) provided by using the above technology for the design of ASIC (Application Specific Integrated Circuit) and a system LSI (Large Scale Integrated Circuit) developed by using the IP that is suitable for embedding systems.

Keywords

single-frame super-resolution, resolution feeling, μPD9245GJ

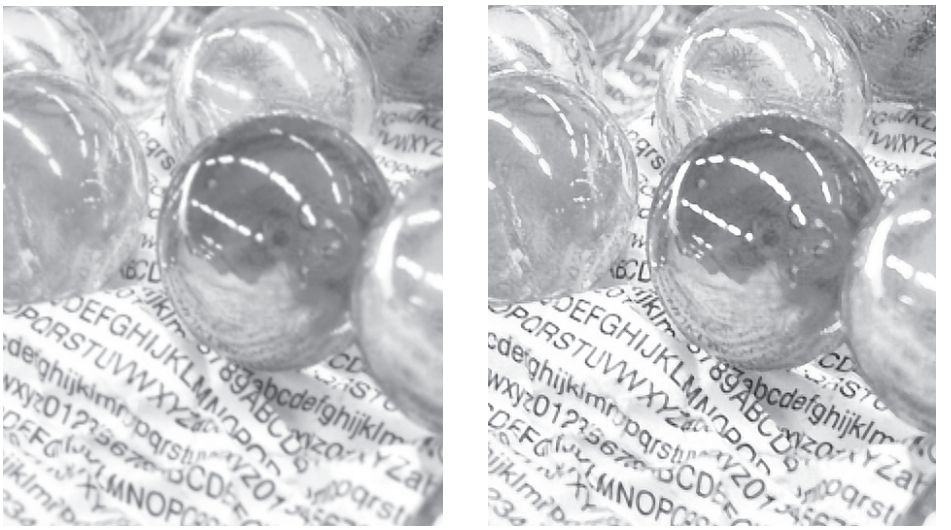
1. Introduction

Recently, the screen size and definition of display devices have been rapidly increasing. A common problem that arises when displaying conventional single-definition image content on a high-resolution panel comes to image blur. This is due to the image magnification process such as bi-linear or bi-cubic interpolation. In order to resolve this issue and to improve the quality of the various images and video easily, we have developed a single-frame super-resolution IP and LSI.

2. Single–Frame Super–Resolution Technology

The "single-frame super-resolution technology" is an image quality improvement technology which removes image blur by analyzing and processing the information present in each frame. More specifically, this technology restores the appearance of blurred contours in images induced by the magnification process. It can thus improve the quality and color reproduction with the sharper image display.

Conventional super resolution techniques improve the



(a) After bi–linear magnification (Area ratio: 4X)　(b) Result of single–frame super–resolution processing

＊See also the color pages in the infographic topping.

Photo 1　Processed images.

image resolution by extracting high frequency component of an image by processing multiple sequential frames. These techniques, however, require external large-sized memory since they have to temporarily store multiple frame images to be analyzed. This constraint imposes delays in processing and increases the current consumption, mounting area and cost. In addition, the multiplicity of processing also poses other issues such as a difficulty in implementing the technique in hardware with a real-time processing capability. Therefore, in order to enable sharp image displays with less data analyses, we have shifted the goal from improving resolution to improving subjective measure called "resolution impression," and in collaboration with NEC Central Research Laboratories, we have developed a new algorithm for super-resolution image processing using a single image frame.

Photo 1 shows an example of the result of single-frame super-resolution processing. Photo 1(a) is the image with blur obtained by bi-linear magnification of the source image with magnification ratio of 4X, and Photo 1(b) is the result of single-frame super-resolution processing using Photo 1(a) as an input. The effect of the process can be observed in sharper edges, improved character legibility and enhanced gloss on the surface of the balls.

3. Single–Frame Super–Resolution IP

The super-resolution IP applying the new technology requires processing of a relatively small amount of data because it can improve the image quality from a single image frame, and it does not need an external memory or software for processing. In addition, it is also capable of processing moving images in real time. The data output interface uses a widely distributed video interface, so embedding in existing systems is easy. As a result, incorporating the IP in a video component that magnifies low-resolution movie and still images in order to display them on a large-screen panel makes it possible to improve the displayed image quality in a short period and at low cost without modifying the system configuration.

The single-frame super-resolution IP offers the following features (see **Table 1** also).

(1) Extremely Light Processing at Low Cost
The technology is implemented fully in the hardware and does not need an external memory (SDRAM/DDR) or software. The circuit is small-sized, can be implemented at a very low cost, and is optimum for embedded applications.

Table 1 IP function table.

Item	Details
Control interface	AMBA bus (APB bus) or direct terminal control
I/O signal formats	YUV input, YUV output. Compatible with max. 16-bit accuracy.
Sub-sampling	YUV 4:2:2 or YUV 4:4:4
Pixel size	Movie: Max. 1,920 x 1,080 (Full HD), min. 320 × 240 (QVGA) Still image: Max. 8,192 x 8,192, min. 128 × 128 or 160 × 120 (QQVGA)
Built-in memory	SRAM (No external memory required)
Operation clock frequency	Max. 150MHz (@ full-HD operation)

(2) Real-time Processing of Full HD Movie (1080p)
The super-resolution processing is executed in synchronization with the dot clock (max. 150MHz). As the output latency is reduced to as low as a few lines, even full-HD movies can be processed in real time without there being concerns about processing delay or audio synchronization.

(3) Little S/N Deterioration Compared to Existing Sharpness Technologies
The image quality is improved while minimizing the noise enhancement effect that tends to occur with ordinary edge enhancement processing.

(4) Easily Embedded in Customers' Existing Systems
The standard YUV interface is used so that the IP can be connected easily to customers' existing systems without the need for system modification.

4. Single–Frame Super–Resolution LSI

We have developed the μPD9245GJ to demonstrate the possibilities of the single-frame super-resolution IP with the 150μm process. This LSI is compatible with a maximum number of pixels up to SXGA (1,280 × 1,024 pixels).

The design concept enables ease of use for all by using a simple add-on procedure to existing systems. In addition to the consideration of operability, the LSI was also implemented with simplified specifications, so that it is easily applicable to either newly developed or existing systems.

Fig. shows the block diagram, **Photo 2** depicts the chip and **Table 2** details the features. The LSI uses the I^2C interface as the host interface and enables various initial settings and image adjustment parameter settings.

Considering that a large variety of color formats such as the

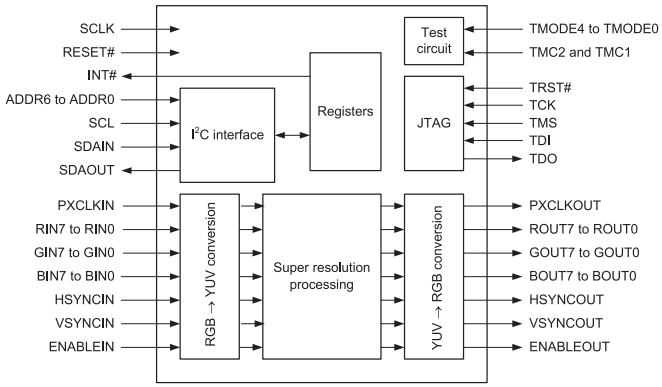


Fig. Block diagram.

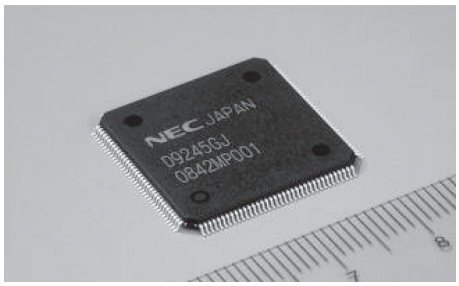


Photo 2 Chip appearance.

Table 2 Features of µPD9245GJ.

Item	Details
Control interface	I²C bus
I/O signal formats	RGB/YUV (ITU-R BT.709/601 color converter built in) Color (8-bit)
Sub-sampling	YUV 4:2:2 or YUV 4:4:4
Pixel size	Movie: Max. 1,280 × 1,024 (SXGA) Min. 320 × 240 (QVGA) Still image: Max. 8,192 × 8,192 Min. 128 × 128 or 160 × 120 (QQVGA)
Operation clock frequency	Max. 108MHz (@ SXGA 60 fps)
Other	Auto image size acquisition
Package	144-pin LQFP, mold size 20 × 20mm
Supply voltage	IO power: 3.3V. Core power: 1.5V.

YUV (or YCbCr) of television systems and the RGB of information equipment, the LSI incorporates a color converter circuit and switching mechanism to deal with the various interfaces used by them. It also incorporates an auto image size identification circuit to facilitate the setting of the number of pixels. The desired number of pixels may also be set by means of register setting. However, the LSI does not incorporate an up-scaling circuit. This is because existing systems already incorporate equivalent functions, that is, there is no need to incorporate these functions double, and we believe that it is important for an embedded system to avoid increased power consumption.

5. Evaluation Board

To facilitate image evaluation, we have fabricated a board mounting the µPD9245GJ (**Photo 3**). This is a small-sized (90 × 50 × 23mm) board that assumes use as an embedded system. It can handle DVI-D signal (RGB signals) and enables evaluation of actual single-frame super-resolution images when it is connected between an image output device such as a DVD player or PC and a display monitor. The board also incorporates a USB control circuit. It is basically powered by the power from the bus but is also equipped with a power connector for use in supplying auxiliary power in a low-power environment such as for operation with a notebook PC.

6. Conclusion

In the above, we have described the single-frame super-resolution IP that enables easy image improvement and a single

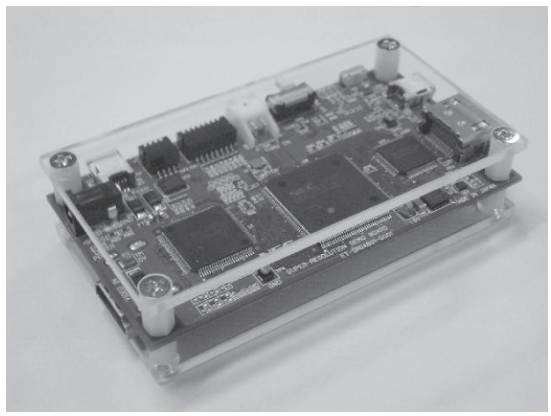


Photo 3 Evaluation board.

frame super resolution LSI (μPD9245GJ) that uses the IP. As its name implies, the single frame super resolution IP performs super resolution processing using a single image frame, so its improvement effect is limited. However, the improvement in the effects enabled by an input image with a low-bit rate still remains as an issue to be solved. In the future, we intend to develop new single frame super resolution IPs and super-resolution LSIs by expanding the scope to lower bit rates in pursuit of further image quality improvement.

It is expected that super-resolution technology will continue to attract attention from the wide range of fields that handle images. We therefore intend to continue device development as of a unique technology that our competitors are not able to imitate.

*ARM is a registered trademark of ARM Limited.

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