LSI and Circuit Technologies of the SX-9

TANAHASHI Toshio, TSUCHIDA Junichi, MATSUZAWA Hajime
NIWA Kenji, SATOH Tatsuo, KATAGIRI Masaru

Abstract

This paper outlines the LSI and circuit technologies of the SX-9 as well as their inspection technologies. NEC Corporation has developed its advanced CMOS technology jointly with NEC Electronics Corporation for use with the SX-9 and has also developed a high-speed interface technology for ultra-high-speed data transfer, high speed and low skew clock distribution technologies and noise reduction and inspection technologies for use in the inspection of the above.

Keywords

CMOS, SerDes, MIM, noise

1. Introduction

The previous SX Series achieved high performance and improved cost efficiencies by means of integration scale enlargement using CMOS technology and the use of parallel processors.

In order to implement even more impressive performances with the SX-9, we have advanced the LSI and circuit technologies further. Since an increase in the inter-LSI signal transmission speed is critical for improving the system performance, we have also developed a new multichannel serial interface for high-speed inter-LSI data transfer for the SX-9. Moreover, both the power consumption and the amount of interface circuitry have been reduced in order to enable the mounting of multiple channels on an LSI.

The improvement of the processing capability of a high-speed system requires an increase in the speed both of the intra-LSI and the inter-LSI signal transmissions. The power noise countermeasures that hinder increases in signal speed are also an important factor. In order to transmit signals stably at high speeds the SX-9 uses wiring boards made of low-loss materials with low signal attenuation during transmission and some of its circuits incorporate an equalization function to improve the transmission signal waveforms. With regard to the increase in power noise that occurs as a result of the increased time of supply current changes due to the use of higher-speed transistors the SX-9 reduces power noise by optimizing the number of decoupling capacitors, etc.

2. LSI Technology

Table and **Photo 1** respectively show the specifications and external view of the CPU chip of the SX-9.

The common specifications of the LSIs used in the SX-9 include the 65nm CMOS process, 11-layer copper wiring, improvements in routing delays by adopting inter-layer dielectric films, etc., implementation of large-capacity on-chip capacitors by developing the MIM (Metal-Insulator-Metal) process and implementation of a high-performance low-voltage supply by reducing the gate oxide film thickness. Low transfer latency is also achieved by developing a new multichannel serial interface.

2.1 Serial Interface

We have developed the SerDes technology with a transmission rate of 10Gbps. Although it is more usual to employ optical

Table CPU chip specifications.

Item	CPU Chip
Technology node	65nm
Number of transistors	350M
Supply voltage	1.0V
Number of pins (signal pins)	8,960 (1,791)
Wiring layer configuration	11 copper layers
I/O interface	CML
Packaging	Bare chip configuration

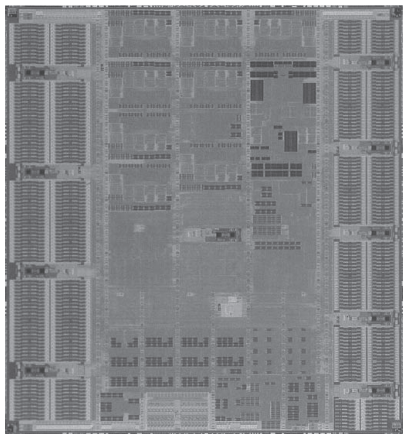

Photo 1 External view of CPU chip.

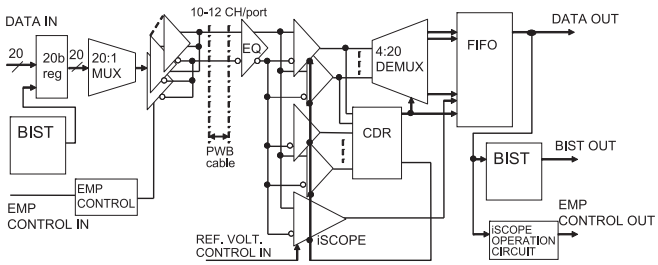

Fig. 1 Multichannel serial interface.

transmission for ultra-high-speed serial interfaces, we developed an electric transmission technology for connecting multiple channels between LSIs.

As the signal is attenuated to about 1/10th due to the waveform distortion produced by the frequency characteristics of the PWB (Printed Wiring Boards) and the cables in the transmission paths, we incorporated a pre-emphasis (EMP) circuit in the transmitter (TX) and an equalizer (EQ) circuit in the receiver (RX). In addition, a sampling oscilloscope (iSCOPE) function is incorporated in RX in order to enable eye diagram sampling of the receivable voltage and timing while RX is mounted in the system (**Fig. 1**).

The input voltage is compared to the reference voltage by using the iSCOPE function, high/low information and the data values before and after the compared data are computed.

The obtained EMP control outputs are then sent to the diagnostic processor. These signals are used, when the system is initialized in order to create the EMP control signal reflecting the degree of data effects before and after the compared data to pre-emphasis of TX and the iSCOPE function's reference control signal, which are then sent to the SerDes circuit. The eye can be maximized by repeating the adjustment.

TX and RX occupy a small area of 0.31μm ^{2} per channel, and about 400 TX/RX channels are accommodated per LSI.

2.2 Clocks

The distributed clocks can roughly be divided into the clocks for logical circuitry and those for interface circuitry.

The logical circuit clocks are distributed with the 2-step method. The clocks distributed over a wide area are wired using the clock-dedicated thick film wiring layer with low resistance in order to reduce the waveform skew due to low resistance, and are distributed with equal delays based on considerations for the inductance component of the wiring as well as for its RC component. The clocks distributed in a narrow area are distributed with equal delays and the clock skew is reduced by optimizing the driving power of the clock drivers. In addition, to reduce the power consumption a clock gate circuit that multiplies part of the clock as required is adopted.

The interface clocks use the CML (Current Mode Logic) circuitry. The CML circuit uses differential signals and drives at a constant current, so that it can increase the clock frequencies and greatly reduce clock jitter due to power noise compared to the CMOS inverter circuit.

In order to generate high-speed clocks, the SX-9 adopts the APLL (Analog Phase-Locked Loop) circuit that multiplies the clock input from outside the LSI. The APLL incorporates LC tank type VCO (Voltage-Controlled Oscillators) composed of inductors and variable capacitances that are fabricated on the LSI and generates a clock obtained by aligning the phases of the external and internal clocks of the LSI. For countermeasures against power noise, a power regulator is built in to reduce jitter by generating the LSI-dedicated independent power supply inside the LSI.

3. High–Speed Circuit Technology

Improvement of the processing capabilities of a high-speed system necessitates an increase in the inter-LSI signal transmission speed as well as in the intra-LSI signal transmission speed. The countermeasures against power noise that hinder increases in the signal transmission speeds are also important.

3.1 Transmission Technology

Inter-LSI signal transmission attenuates the high-frequen-

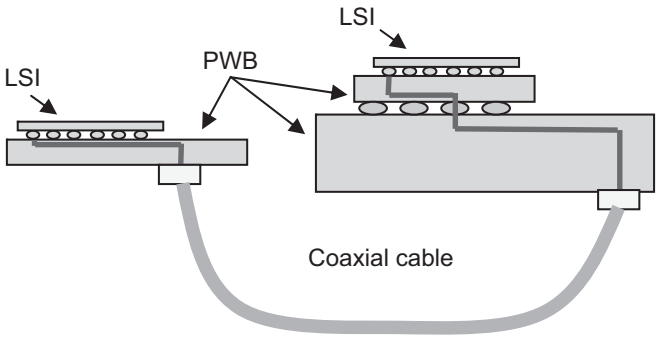

Fig. 2 Inter-LSI connection configuration of SX-9.

cy component of a signal due to the skin effect and the dielectric loss of the transmission path. This makes correct signal reception impossible when the wiring length is long.

As shown in **Fig. 2** , the structure of the inter-LSI connections of the SX-9 tends to increase the attenuation because of the connections between the multiple wiring boards. A pre-emphasis function has been added to ensure correct signal reception in such a transmission path structure. The pre-emphasis function was also used with the SX-8 but it has been enhanced for the SX-9 by increasing the number of amplitude adjustment steps and by introducing an algorithm for the automatic setting of the optimum step value according to the results of received waveform monitoring.

In addition, the wiring boards are made of low-loss materials with low signal attenuation and low-loss cables for connection between the wiring boards that have been newly developed to reduce the overall attenuation via the transmission path.

When we had decided on the transmission channel structure, we simulated the transmission path and evaluated the LSIs for use in testing.

With the transmission path simulation, we introduced a system for modeling the 3D structure of the wiring board based on electromagnetic field analysis in order to improve accuracy by the use of high frequencies. Using the electromagnetic field analysis simulator, we varied the conditions of the wiring board such as the wiring length, via holes and pad shape and implemented a transmission path structure that could offer an eye aperture of the reception waveform matching the design target.

We also compared the reception waveform obtained by the transmission path simulation to the reception waveform after transmission via the actual transmission channel, and confirmed that the simulation was correct and accurate. **Fig. 3**

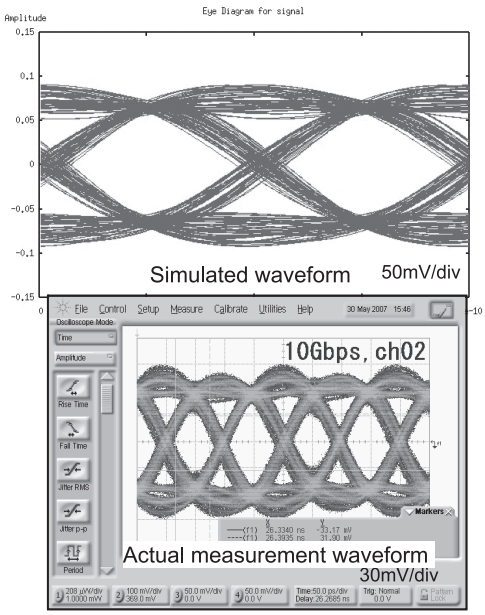

Fig. 3 Simulated waveform vs. actual measurement waveform.

shows the simulated waveform and the actually measured waveform.

The inter-LSI transmission with the path structure as shown in Fig. 2 has been implemented based on the studies and verifications as outlined above.

3.2 Power Noise Countermeasures

In order to achieve ultra-high-speed transmission, it is necessary to adequately reduce power noise, decrease the jitter superimposed on the transmitted waveform and ensure the margin of the circuit operation. With the SX-9, we have quantitatively identified the degree that the power noise generated in the core logic circuit is propagated to the ultra-high-speed I/O by carrying out an integrated analysis from the wiring board to the LSIs. As a result we were able to determine the value of on-chip capacitance mounted in the LSIs so that the amount of propagation does not affect the SerDes circuits.

However, as we could not reserve a sufficient capacitance value for the SX-9 with the capacitance created using the gate, we placed MIM capacitance on the highest layer of the LSI so that the MIM capacitance is uniform all over the chip surface in order to enable efficient and effective noise reduction. The use of the MIM capacitance makes it possible to reduce the amount of noise over a wide range of frequency bands. **Fig. 4** ,

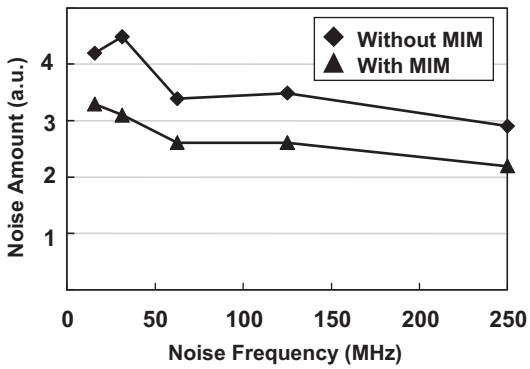

Fig. 4 Results of MIM capacitance evaluation.

which plots the results of measurements of noise amounts when the MIM capacitance is used or not used by using frequencies as the parameters, demonstrates that the MIM capacitance is actually capable of reducing power noise over a wide range of frequency bands.

We measured the actual effects of the noise reduction measures by mounting noise and jitter measuring circuits on the LSI and applying the specified amount of jitter using a clock modulator, and confirmed the reservation of a margin in the inspection.

4. Inspection Technology

4.1 LSI Test

The LSI test conducted for the SX-9 achieved a high detection rate by adopting BIST (Built-In Self Test) circuits that can function at the actual operation speed in addition to the scan path method that has been adopted since the previous model. The BIST circuits are generally used widely with memory circuitry, but we have developed an original BIST circuit for the logic circuitry in addition to the BIST circuit for memory and have incorporated it in the SX-9. We have designed the BIST circuits so that they can test the CPU by dividing it into circuits in order to reduce the power consumption for LSI testing. This procedure has solved the problem of the restriction of power capacity of the LSI tester.

4.2 Module Test

Since the SX-9 uses a large number of RAMs, the RAM inspection is as important as the LSI inspection. In the testing of modules incorporating RAMs, we have developed a special inspection system at the actual operation speed for the RAMs in each module. We also incorporated the RAM test function in the LSIs in each module to reduce the inspection equipment cost.

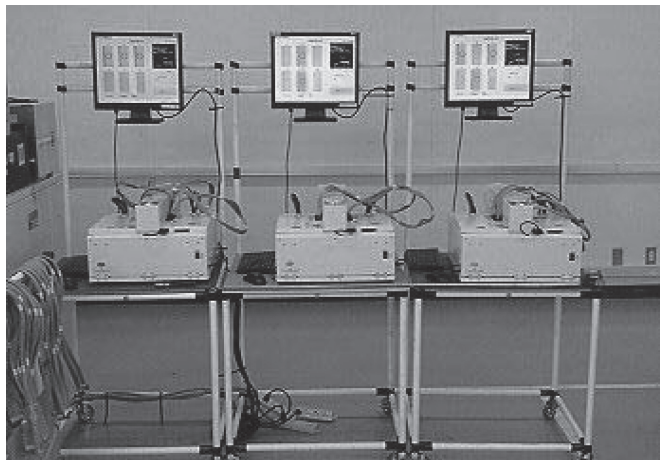

Photo 2 External view of the cable inspection system.

4.3 Coaxial Cable Test

The SX-9 uses coaxial cables for inter-module transmissions, but the traditional conductivity inspection is inadequate for ensuring stable transmission of signals at the high speed of 10G bits/sec. However, it is also unrealistic to measure detailed electrical characteristics considering the long time that would be required for such inspections. Therefore, we have newly developed a cable inspection system for the SX-9 (**Photo 2**). This inspection system actually transfers data at 10G bits/sec. and measures the error rate while guaranteeing high quality. The error rate measurement is carried out by a measurement-dedicated LSI to reduce the measurement time.

5. Conclusion

In the above, we have summarized the outlines of the LSI, circuit and inspection technologies for the SX-9. In the future, we intend to develop more LSI and circuit technologies so that we can implement supercomputers that offer high performances at appealing prices.

LSI and Circuit Technologies of the SX-9

Authors' Profiles

TANAHASHI Toshio
Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

TSUCHIDA Junichi
Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

MATSUZAWA Hajime
Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

NIWA Kenji
Assistant Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

SATOH Tatsuo
Executive Expert,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

KATAGIRI Masaru
Executive Expert,
Computers Division,
1st Computers Operations Unit,
NEC Corporation