Platform Technology Achieving Size Reduction, Power Saving and High Performance

HOSOI Toshikatsu

Abstract

The platforms for mobile terminals are advancing daily in pursuit of the need to increase the number of functions and improvements in performance. The items required for the platforms are not only to support the advancement of function and performance but also include basic performance functions that are critical for the mobile phone, such as size reduction and power saving. The new platform adopted for the FOMA (R) N905i has succeeded in meeting these requirements by adopting new technologies and achieving size and power consumption reductions at the same time as integrating a multiplicity of function and high performance improvements. This paper introduces the latest mobile terminal platform and the technologies employed by it.

Keywords

cellular phone, platform, baseband, application processor, W-CDMA, HSDPA, GSM, power saving

1. Introduction

The FOMA N905i released in November 2007 uses the Medity2 (general-purpose LSI of NEC Electronics) to achieve both high performance and low power consumption as well as a newly developed power management unit that is dedicated exclusively to the power optimization of the Medity2. The main chipset features a significant reduction in the component packaging area thanks to the integration of the baseband and application processor blocks that have previously been provided in two chips. The new platform also incorporates other innovative peripheral devices by providing multiple high-performance functions. These include; an overseas roaming capability using the GSM communication core, a high-speed downloading capability using the HSDPA communication core and a CPU with the highest speed among FOMA of 500MHz [*1] . All of this is now available with low power consumption similarly to the previous platforms. In the following this paper will describe the features of the new platform and the technologies adopted by it.

2. Summary of the Incorporated Functions

One of the most significant features of the Medity2 is the minimized packaging area, which has been made possible by integrating the functions of the baseband, application processor and the peripheral devices in a package size equivalent to that of a traditional application processor. For the communication functions, the GSM communication core is added to the W-CDMA core to enable communications in more than 150 countries that are not currently covered by 3G roaming, these include the USA and China. The HSDPA 3.6Mbps communication core is also added to enable high-speed downloading with a single chip (**Fig. 1**). The functions incorporated in

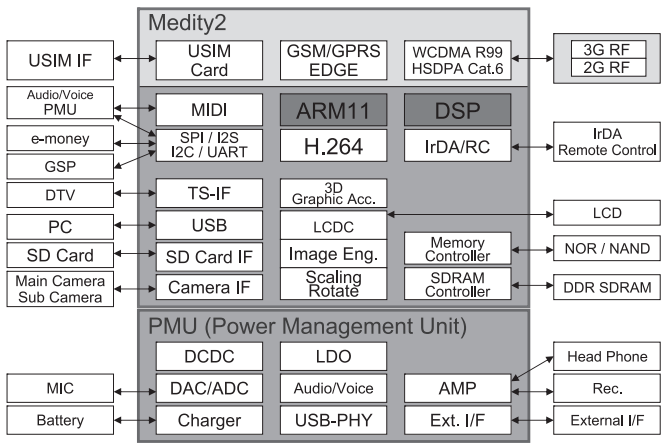

Fig. 1 Block diagram of new platform.

[*1] As of November 2007.

Medity 2 are as follows:

1) Digital Baseband Block
- W-CDMA Release 99
- HSDPA Cat. 6 (3.6Mbps)
- GSM/GPRS/EDGE Class 12

(N905i, N905iμ and N705i: Class 5, EDGE incompatible)
(N705iμ: GSM/GPRS/EDGE incompatible)
- USIM Interface

2) Application Processor Block
- CPU: ARM11 500MHz, L1/L2 Cache
- DSP: K7 500MHz, L1 Cache
- SDRAM controller: DDR 32-bit, 166MHz
- Memory controller: 16-bit, 83MHz, NOR/NAND
- 128-tone sound source
- LCD controller: Max. WVGA, 260,000 colors
- Image synthesis/enlargement/reduction/rotation/color space conversion engine
- 3D Graphic Accelerator

- 2M triangle/sec. or more, Open GL ES 1.0/1.1
- H.264 Encode/Decode engine
- (micro) SD Card Interface
- TS-Interface,USB (High-Speed/Full-Speed)
- Various serial interfaces

The integration of multiple functions as seen above has made it possible to provide mobile terminal functions from a single chip. Additionally, a 500MHz CPU and an image processing engine featuring image synthesis, enlargement and reduction capabilities are also incorporated in order to process 4 times more data than before at a speed that will not cause stress in the user interface even with a large WVGA (Wide VGA) sized screen. The multimedia processing uses a 500MHz DSP and the H.264 hardware engine for compatibility with various movie formats including recording and playback of D1 (720 × 480) size movies, and viewing, recording and playback of terrestrial digital broadcast TV.

3. Size and Cost Reduction

With the N904i, the total area of four LSIs including 1) application processor, 2) digital baseband, 3) HSDPA accelerator and 4) sound source was 475mm ^{2} . Meanwhile, the N905i using the Medity2 chipset has integrated the four LSIs into a single chip by means of process shrinking, and has reduced the component package area to 196mm ^{2} , which is about 41% of that of the previous device. Also, the three power LSIs have also been integrated into a single LSI, achieving a reduction of about 42% in the packaging area. These LSI integrations have reduced the total packaging area of the chipset by 56% from 604mm ^{2} to 263mm ^{2} , thus contributing to the implementation of compact/slim mobile terminals such as the N905iμ and N705iμ (**Fig. 2**).

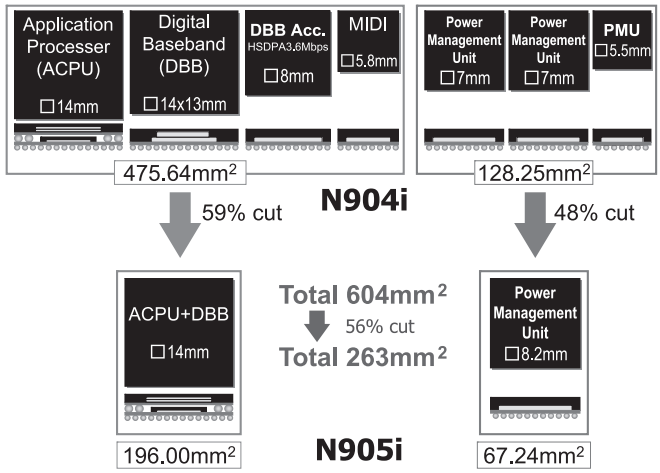

Fig. 2 Comparison of LSI configurations between N904i and N905i.

In addition to the packaging area, the total cost has also been reduced by implementing modifications of the following four points; 1) reduction of the device cost thanks to process shrinking and one-chip implementation; 2) reduction of the number of DRAMs from three to two by sharing a DRAM between the baseband and application processor; 3) improved yield by changing the package configuration from SIP (System In Package) to POP (Package On Package) to separate the DRAMs and processors into two packages; 4) purchase of a lower-priced memory by increasing the memory manufacturer options thanks to the use of POP package configuration.

4. Low Power Consumption

The mobile phone is subject to the need to improve processing performance in order to deal with an increased number of functions such as a larger screen, Java applications including games and browsing with high-speed communication. However, improvements in function and performance tend to increase the device power consumption and this makes improved power saving measures more desirable. To solve this problem, it is important from the perspective of the system design for a mobile phone to enable a reduction in power consumption at the architecture level by introducing new

technologies. As the actual issues lie in how to extend the standby time and the application operation time, the power saving design is a design consideration that is quite as important as the designs of function and performance. The following section introduces a summary of the power saving technology as the key technology in mobile phone design.

4.1 Outline of the Power Saving Technology

The power consumed by a device can be divided roughly into the operational power and the leakage power. The leakage power is dominant in the standby mode, and the operational power is dominant in the operation of applications for talking and mailing.

The change from Medity1 to Medity2 has increased the circuit scale to 200% and the bus frequency to 130% and the total operational power would be increased to 260% if power saving measures were not implemented. With regard to the leakage power, this doubles when the circuit scale is doubled. If the power consumption were left increased following the improvement of function and performance, the actual time available for the mobile phone would shorten considerably. In order to avoid this, it has been an important issue to reduce the power consumption to a level equivalent to that of Medity1 by utilizing power saving technologies.

This issue has been solved by reducing the operational power to 70% of the possible increase of 260%, or to 180% by means of process shrinking and by then reducing it even further to the Medity1 equivalent level by means of quick recovery and clock control technologies. We have also reduced the leakage power to the Medity1 equivalent level by reducing it with the combined effects of the use of multi-Vt transistor configuration, separation of power supply, incorporation of a power switch and improvement to the DC-DC converter efficiency (**Fig. 3**). The following sections discuss these innovative technologies that have been adopted for the Medity2.

4.2 Quick Recovery

When the CPU stops, the quick recovery technology reduces power consumption by automatically saving the CPU status and then turning the power supply off. The high-performance 500MHz CPU uses a large number of high-speed transistors, so the leakage power becomes 10 to 100 times higher than for the low-power process and a wasteful current of the order of tens of milliamperes would continue to flow even after the CPU clock has stopped. The wasteful current

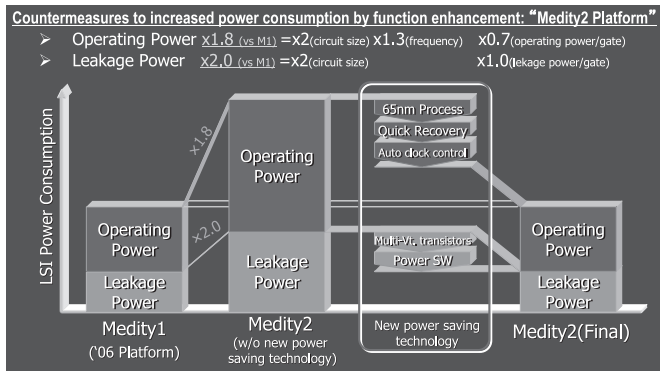

Fig. 3 Outline of low power consumption technology.

consumption is usually avoided by switching the CPU power off, but this resets the CPU register to the initial state so the CPU status would become the same status as after startup from reset when it recovers from interrupt. To prevent this happening, the CPU saves the register status, etc. in the memory before the power is switched off and recalls the saved status in recovery after power on. In fact, with the previous Medity1 platform the CPU performed both the save and recovery processing operations.

However, as the previous method consumed excessive power for saving and recovery operations, its current reduction effect was small for applications with a low operational current such as music playback. In addition, the method also had other disadvantages, such as the problem of the response rate due to delays in the interrupt recovery time and the labor required for verification during software development. The innovative quick recovery technology adopted by Medity2 and implemented by automation of hardware solves the above problems by performing the status save/recovery operations at power off/on, which has hitherto been processed by software in the Medity1 platform.

4.3 Clock Control

The Medity2 platform uses two clock control functions including the clock On/Off control and an auto frequency control. It performs fine On/Off controls to supply the clock only to the necessary circuitry and at the necessary timings.

The clock On/Off control can be divided into the gate control of the clock on a per-function macro basis and the gate control of the finer clock in the hierarchy inside each macro. These two kinds of gate control contribute to an operational power reduction by reducing the operating clock to the mini-

mum required level.

The auto-frequency control automatically decreases the overall operating frequency of the chip to a predetermined frequency when the CPU and DSP do not need a high operating frequency during standby. This resulted in the reduction of the overall operational power of the chip. This function can reduce the base current and achieves an overall chip power saving effect of 20% to 30%. As this function is more effective when the processing time of the application is shorter, the use of the high-speed 500MHz CPU/DSP can reduce the processing time further and also improve the power saving effect. In fact, it has already been confirmed that applying auto-frequency controls to operations at the highest speed is more effective for power saving than decreasing the operating frequency.

4.4 Multi–Vt Transistors

The multi-Vt transistor technology reduces the leakage power by using three kinds of transistors, for the low, medium and high speeds, according to purpose. The leak current with the middle-speed transistor is 10 times higher than that of the low-speed transistor, and the leak current with the high-speed transistor is 100 times higher. Low-speed transistors are suitable for circuitry usually switched on all day which is employed for mobile equipment and are mainly used in the baseband circuitry. Medium-speed transistors are used in parts where the speed is inadequate when low-speed transistors are used. High-speed transistors are used in CPUs and DSPs and are switched off when not in use. The advantages of using the high-speed transistors include the possibility of using the high-speed 500MHz CPU as well as the power saving that results from combination with the built-in power SW.

4.5 Power Switch and PMU Configuration

The previous Medity1 platform required a dedicated power supply for each power domain inside the LSI, and the use of a regulator ([REG] in **Fig. 4**) in the latter stage of the DC-DC converter hindered the efficient use of power. This problem has been solved with Medity2 by reviewing the power supply configuration.

We integrated the power domains with a low current reduction effect between standby and operation, and provided the other power domains with internal power switches. Specifically, the L0/DBB/MEMC domains are integrated into a single domain that is permanently switched on, and a switch is built into the L1 domain to switch it off during standby. The power

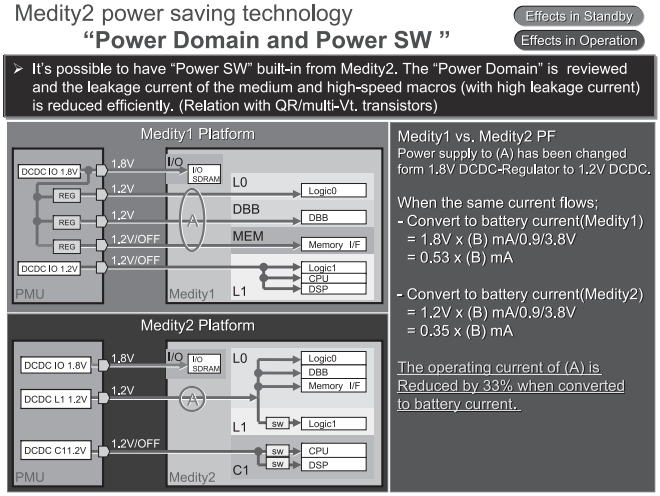

Fig. 4 PMU and power switch configuration.

supply configuration has also been reviewed to separate the CPU and DSP into different domains and incorporate power switches in them so that the DSP can be switched off when it is not used and to enable the DC-DC converter to be also switched off when the CPU and DSP are not used. Incorporation of a switch in each power domain enables direct drive from the DC-DC converter and can therefore reduce power consumption. As a result of the review of the power supply configuration, we have succeeded in power saving of more than 33% when converted into battery power (Fig. 4).

As described in the above, in spite of the power consumption being increased due to doubling the circuit scale, the performance was improved. We also succeeded in achieving an operational time that was practical for mobile phone use by reducing the power consumption to a level equivalent to that of the Medity1 platform. This was achieved by means of integrating the four innovative technologies of; 1) quick recovery; 2) clock control; 3) multi-Vt transistors; 4) power configuration review and power switch incorporation. In addition, a significant process shrinking method contributed to the achievement.

5. Conclusion

The enhancement of market appeal by the addition of functions and performance improvements has posed problems such as increases in the circuit scale and power consumption to the mobile phones. In order to deal with these problems and with

future sales perspectives in mind, we have developed a platform that can serve the implementation of truly competitive products by incorporating innovative size and power consumption reduction technologies.

In closing, we would like to express our gratitude to Ricoh, Ltd., for their cooperation in the development of the platform introduced in this report.

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Author's Profile

HOSOI Toshikatsu
Senior Manager,
Mobile Terminals Platform Development Division,
Mobile Terminals Products Development Operations Unit,
NEC Corporation