The “CB-55L” a Low Power Consumption 55nm Cell-Based IC Product

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Abstract

The CB-55L is a cell-based IC product based on a 55nm process that adopts various techniques for reducing the lead time and cost of development.

Circuit design techniques such as process miniaturization are featured in order to reduce power consumption. This paper introduces the design procedures aimed at meeting the requisite functions of the CB-55L, which is a cell-based IC product that has successfully developed with a short lead time.

Keywords

CB-55L, 55nm process, cell-based IC, low power consumption, large-scale integration, large-scale design

1. Introduction

Product development in the digital consumer market follows firmly established trends such as the provision of full-HD compatibility for flat-panel TVs and improvements in the product functions and performances of cellular phones. As a result the LSIs used in these products are required to have their scale and integration functions increased even more.

In the case of battery-powered portable products such as cellular phones, the battery operating period has also become an important issue that imposes a demand for power consumption reductions on the LSIs used in these products. In addition, a reduction of power consumption is also required for non-battery-powered equipment due to the recent rise in concerns about environmental issues.

Targeting mainly the development of ASICs for use in digital consumer products, NEC Electronics has begun development of the CB-55L, a cell-based IC product using the 55nm process, and has been receiving market orders since January 2007. Thanks to its increased scale and integration capability the CB-55L offers improvements both in its LSI performance and power consumption characteristics. In the following sections, we will introduce the CB-55L and outline the design techniques that have enabled us to develop a large-scale, low-power-consumption LSI with short development lead time at low cost.

2. CB–55L Product Outline

The CB-55L is the first cell-based IC in the world to use the 55nm process at the mass-production level. An outline of the product is shown in **Table 1** .

The 55nm process employed by NEC Electronics has newly adopted a High-k gate insulation film to reduce leak current and provide compatibility between low power consumption and high transistor performance. It achieves a higher operating speed than the CB-90M/CB-90L series, which are cell-based IC products by using the 90nm process, and it reduces the leak current per gate as shown in **Fig. 1** . With regard to its fabrication technology, it featured an ArF liquid-immersion exposure technique before any of its competitors (**Fig. 2**). This innovation has enabled a reservation of manufacturing margin in the lithography process and a stable supply of products based on these advanced processes.

The CB-55L includes three cell libraries composed of transistors with different threshold voltages (Vt) as shown in **Table 2** . Using the optimum cell library according to the LSI’s

Table 1 CB-55L product outline.

Item	CB-55L Data
Process	55nm CMOS process
Supply voltage (Core logic)	1.0 - 1.2V
Interface level	3.3V, 2.5V, 1.8V
Wiring layers	6Cu + 1Al, 7Cu + 1Al
Applicable packages	PBGA, FPBGA, FCBGA

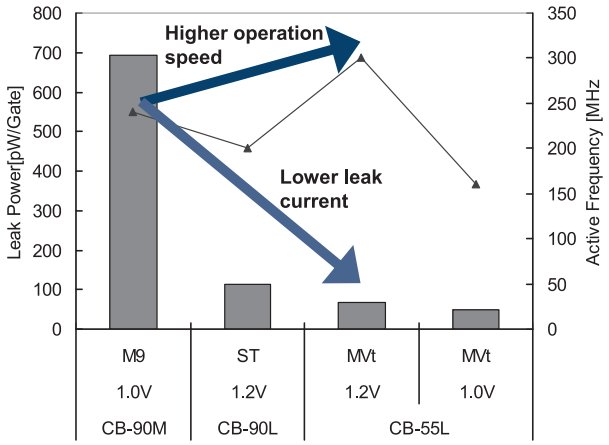

Fig. 1 Operating frequencies of 90nm/55nm standard Vt cells, leak current per gate.

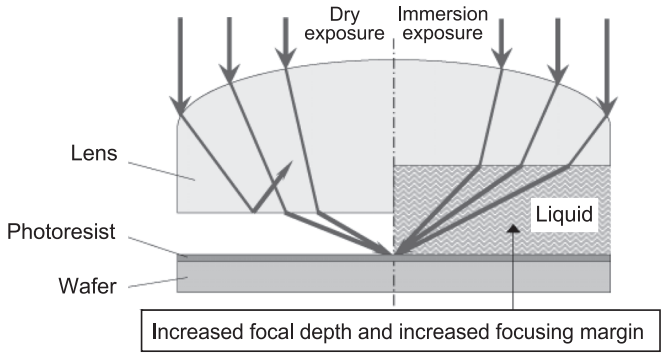

Fig. 2 Immersion exposure.

Table 2 CB-55L cell library list.

Cell name	HVT	MVT	LVT
Threshold voltage (Vt)	High	Medium	Low
Application	Low leak	Standard	High operation speed
Target frequency (High-density version cell)*	220MHz	300MHz	450MHz
(High-seed version cell)*	266MHz	400MHz	600MHz
Supply voltage	1.0-1.2V		

* Operation frequency data in 1.2V operation.

Table 3 Memory cell sizes.

Item	SRAM (High-density type)	eDRAM
Area	0.446μm²	0.124μm²

operating frequency makes it possible to reduce the leak current. The provided cell libraries are compatible with supply voltages from 1.0 to 1.2V. Each cell library includes two versions, one composed of the high-density version cells typically used in design of user logics and the other composed of the high-speed version cells that are mainly used in the design of high-speed macros.

The memory macro using the embedded DRAM (eDRAM) approved for the 90nm products is also available, as well as an SRAM product. The cell sizes of these products are as shown in **Table 3** and are ranked in the top class compared to the 65nm/55nm process-based products that are being released by our competitors. The CB-55L can use all of the core functions, including the cell libraries even when the eDRAM product is used and addition of the eDRAM does not impose any restriction on the timing and layout designs. The user can select the SRAM or eDRAM product flexibly according to the memory size requirement and application of the LSI.

3. Techniques for Power Consumption Reduction

The CB-55L reduces the power consumption not only by improving the process but also by the introduction of other techniques as described below.

3.1 Power Consumption Reduction Using Multi–Vt and Low–Power Consumption Cells

As mentioned above the CB-55L has three cell libraries. The cells with low Vt values are capable of high-speed operation but their leak current is large, whereas those with a high Vt value have low leak current but the operation speed is slow. After completion of the layout design, we replaced the cells mounted in the paths with timing flexibility by cells that have high-Vt in order to reduce the leak current. This strategy has made it possible to reduce the leak current without affecting the design program (**Fig. 3** and **Fig. 4**).

Low-power-consumption cells are designed with the aim of reducing the operating power by decreasing the gate width compared to that of ordinary cells. In addition to replacement by high-Vt cells, we have also replaced the cells mounted in the path with timing margin by low-power consumption cells after completion of the layout design. This has made it possible to reduce the operating power without affecting the timing design.

These multi-Vt cells and low-power-consumption cells have

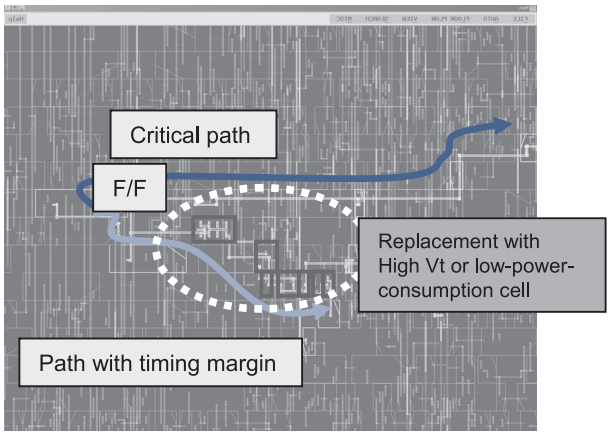

Fig. 3 Example of multi-Vt cell replacement.

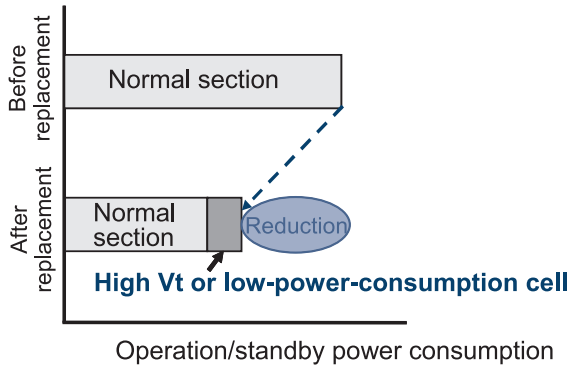

Fig. 4 Example of effect of multi-Vt/low-power-consumption cell replacement.

identical function block layouts, metal wiring shapes and terminal positions to those of ordinary cells, so that they may replace them without wiring modifications. This means that the power reduction can be reduced with a minimum effect on the layout design period.

3.2 Power Consumption Reduction by Clock Gating, Power Supply Separation and Internal Power Switch

In order to reduce the operating power of the LSIs, it is effective to control the clock supply to the circuitry and modules. It is also effective to stop the clock when the circuitry is not working. Similarly to the previous products, the CB-55L also has a clock-dedicated block so that the above design may be easily applied.

Other leak current reduction techniques include ones that separate the power supply or employ an internal power switch (**Fig. 5**). This technique can reduce the leak current by shutting down the power supply to non-operating circuitry and modules. When a power supply separation design is used, a different supply voltage can be supplied per module in order to reduce the aggregate operating power. When an internal power switch design is used, a retention flip-flop may also be used for data retention during the power shutdown periods. The flip-flop is supplied with backup power in order to retain data even when the main power is shut off.

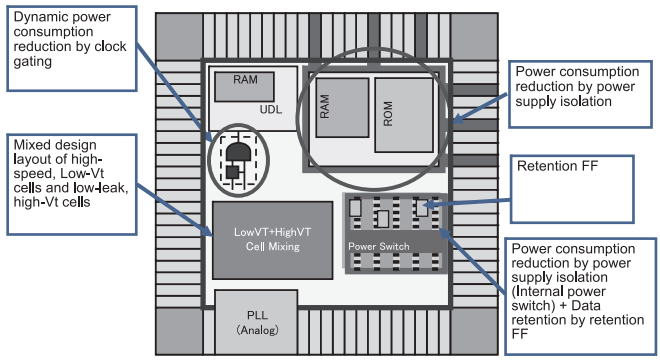

Fig. 5 Example of power consumption reduction design.

3.3 Consistent Design Flow Enabling Low Power Consumption

The power consumption reduction technique using power supply separation or internal power switching described in section 3.2 above has been approved in the design of mobile-use LSIs that are subject to strong commercial pressures to implement power consumption reductions. In this context the technique has already been applied to the designs of some cell-based LSIs. However, when adopting such methods it is required to define the power control specifications in the functional design and to reflect them in the logic and circuit designs. Moreover, it is extremely difficult to achieve consistent design flow because these designs and verifications are more complicated than for ordinary designs and the specifications and methods of power supply control vary depending on the EDA tools used in the flow.

In order to resolve the above issues and meet the various requirements for reducing power consumption in the short period that we had available for the development of the cell-based IC design, we adopted a design flow for the CB-55L based on the CPF (Common Power Format) that complies with the

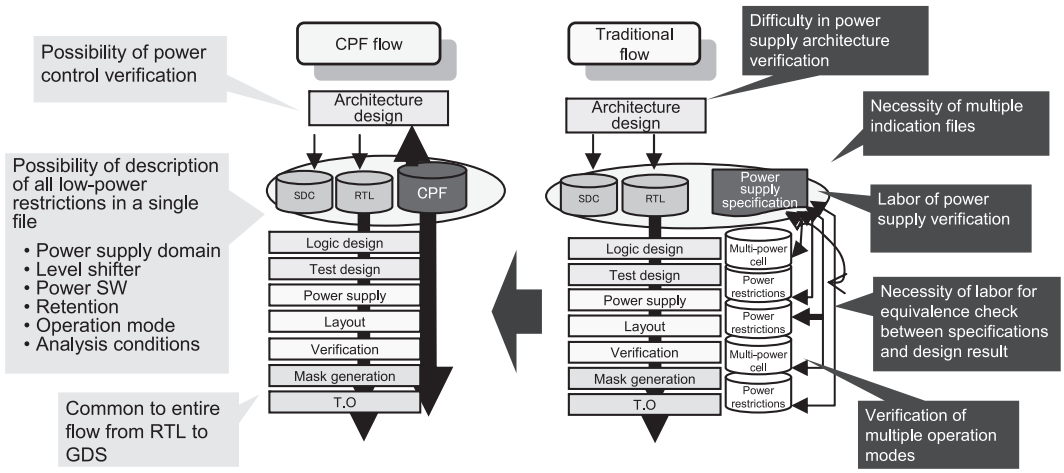

Fig. 6 Example of design flow based on CPF.

standards of the industry standardization organization Si2 (http://www.si2.org/) (**Fig. 6**). This has made it possible for us to implement a consistent power consumption reduction design system that covers logic design to simulations and layout design. Thereby facilitating a smooth design process and enabling a shortening of the development period.

4. Measures for Large–Scale LSI Design

The CB-55L can mount circuitry with more than twice the scale of the circuitry of 90nm-generation products, and the LSIs implemented using the CB-55L are more complicated than before in order to deal with the more demanding performance specifications of the products in which they are incorporated. To design such a large-scale, complicated cell-based IC with a similar design period and cost as before, we have adopted the techniques as described below for the CB-55L.

An increase in the scale and complexity of the LSIs is expected to increase the number of customers requesting ECOs (Engineering Change Orders: Circuit change after design) at the design completion or sample evaluation stage. We have therefore provided the CB-55L with the measures to rapidly facilitate ECOs at low cost.

4.1 Development Technique to Enable a Development Term Reduction

One of the techniques for shortening the layout design period is to arrange the layout design by using temporary-set circuit information at the initial stage of development. This technique enables an early verification of the following items, thus making early feedback to the logic design and chip floor plan and a reduction of the modification period in the post-design process possible.

- Checking the validity and ease of wiring of the LSI floor plan.
- Checking the timings
- Checking the effects of the signal integrity (SI) and power integrity (PI) issues including intra-chip IR Drop and noise verification.

Timings are arranged using our unique timing optimization tool, which enables quick, efficient timing solutions by meeting the various requirements of the advanced process, including considerations for multiple library corners as well as those for SI and PI (**Fig. 7**).

4.2 ECO Facilitation Techniques

In order to easily handle ECOs occurring in the design completion stage at low cost, a procedure that minimizes effects on the development period, the CB-55L adopts the following techniques.

1) ECO Countermeasure Using Dummy Flip-flops

With this technique, dummy flip-flops are inserted in the circuitry in advance in order to deal with ECOs placed at the final stage of design by modifying the already laid-out data wirings. With little backward movement, this technique can

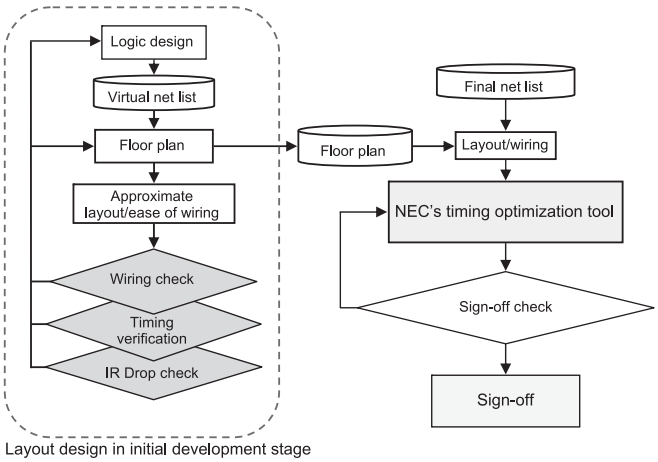

Fig. 7 Development technique for development period reduction.

deal with ECOs without much affecting the development schedule.

2) ECO Countermeasure by Modifying the Metal Wiring Layer Only

This technique can deal with ECOs placed after completion of the design simply by modifying the metal wiring layer. The cost is thus minimized because the mask modification work required for manufacturing is limited to the metal wiring process. This flow implements automation using EDA tools and can modify some tens of circuit points in a few hours. The effect of the sample shipment on the lead time is thus minimized.

3) Timing Closure Process While Carrying out Customer Circuit Modification Requests

In the case where an ECO is placed at the final stage of design, the timing closure process is possible concurrently with the circuit modification work requested by the customer. This procedure will minimize increases in the design period due to circuit modifications.

5. Techniques for Confident Manufacturing of 55nm–Generation LSIs by Reducing the Design Margin

With advanced processes the changes in the characteristics are very high and depend on the process variations. As a result, the traditional design technique of considering variations as design margin may not permit completion of the design process due to the very large margin involved. The CB-55L employs statistical design techniques in order to reduce the margin of the design (**Fig. 8**).

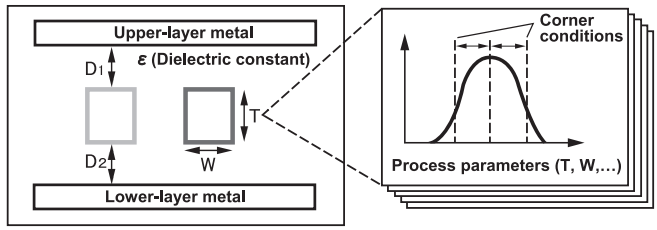

Fig. 8 Statistic capacity/resistance extraction technique.

1) Statistical Capacitance/Resistance Extraction Technique

This technique extracts the capacity and resistance of wiring by considering its shape, and determines the corner conditions for the capacity and resistance values statistically. Compared to the traditional technique that adopts the corner conditions possible for the process directly as those for the capacity and resistance values, this technique can decrease the variation between the Best-Worst delay values and enables practical delay calculations based on considerations based on the actual wiring shape.

2) STA (Statistical Timing Analysis) Considering the Number of Logic Steps

The STA considers variations of LSIs. It can identify the random components in the process variations statistically so that variations may be reduced by considering the number of logic steps in the timing path.

The technique that executes STA automatically by referring to the circuit information of the timing analysis target path is the location-based on-chip variation (LOCV) technique that considers the number of logic steps. It enables considerations on the process variations according to the real circuitry.

3) SSTA (Statistical STA) Technique (Under Study)

This technique handles the delay variation of each cell statistically and compiles it into a library for use in timing analysis. The delay value is not the deterministic value used in the traditional techniques, but is calculated as a value with a statistical distribution. For the CB-55L, we plan to adopt the SSTA technique that is currently under study.

6. Conclusion

The CB-55L makes it possible for cell-based ICs to meet the needs of the digital consumer field in terms of scale, complexity and power consumption reductions. This paper has descri-

bed the CB-55L by focusing on the various techniques used in developing a cell-based IC with a short lead time and at low cost. We are able to provide the requisite services for facilitating the rapid development of cell-based ICs based on the latest 55nm processes at low cost. These solutions are aimed at contributing to the achievement of development programs set by customers.

Reference

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