Development of Baseband LSI (M2) Enabling High-Speed Communication for Handsets

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Abstract

NEC Electronics has developed a baseband LSI "M2" for use in mobile handsets that consists of a single chip incorporating both a high-performance baseband function that corresponds to HSDPA of W-CDMA and GSM/GPRS, and an application processing function. The M2 is based on the advanced 65nm process technology, and features various technologies designed to reduce power consumption. These technologies are applied in the circuit and layout designs to achieve an increase in speed and a reduction in power consumption at the same time as a reduction in the chip size.

Keywords

W-CDMA, baseband, mobile handset, application, power consumption reduction

1. Introduction

Since the start of the service in 2001, the UMTS (Universal Mobile Telecommunications System, which is known as the W-CDMA: Wideband Code Division Multiple Access in Japan) has spread and expanded steadily as the "third-generation cellular phone." However, it remains subject to prevailing market functions and ongoing quality improvements. This has made it necessary to process various advanced applications, to handle a large amount of data and to hold large-capacity communications at high speed. This paper describes the development of the LSI (M2) in pursuit of high performance, multiple functions and low power consumption suitable for cellular phones.

2. Background to the M2 Development

The methods of high-speed, large-capacity communication used by W-CDMA are HSDPA (high Speed Downlink Packet Access) and HSUPA (High Speed Uplink Packet Access). The LSI therefore needs to incorporate these functions.

The key to the diffusion of mobile handsets is their worldwide deployment and this requires compatibility with the GSM/GPRS (Global System Mobile communication / General Packet Radio Service) infrastructure that is already functioning worldwide. A dual function roaming capability enabling W-CDMA and GSM/GPRS is also an important consideration. In addition, from the viewpoint of applications, mobile handsets are also required to mount advanced functions such as a high-speed/high-definition image processing capability and a terrestrial digital TV broadcasting compatibility. However, these requirements conflict with the power consumption requirements of mobile handsets because the LSI must feature high-speed processing and large-scale circuit integration in order to provide optimum performance and function requirements. In this context, the means of reducing power consumption has become a critical issue.

In addition to improvements in performance and functions, mobile handsets are also required to have reduced package sizes in order to reduce device mounting areas. It was based on the above background that we started development of the baseband LSI (M2), which incorporates complex functions with low power consumption and a compact size optimized for use in cellular phones.

3. Targets of the M2 Development

M2 is an LSI featuring advanced baseband and high-performance application processing functions. It has been developed by setting the following functions and performances as the targets.

- Incorporation of the HSDPA and HSUPA interface functions.
- Incorporation of the GSM/GPRS functions for dual operation.
- Improvement of the CPU and DSP performances for more advanced image processing.

- Incorporation of a sound source function.
- Low power consumption equivalent to that of the M1 previous product.
- PoP (Package on Package) structure enabling lamination of commercially available memory chips.

4. Architecture of the M2

M2 features additional functions and an enhanced performance compared to the applications to the previous M1 product (**Table**), and its architecture incorporates the GSM/GPRS and HSDPA functions in the baseband block. **Fig. 1** shows the block diagram of the M2.

The architecture of the M2 has the following features.

- The AHB and AXI buses are employed to reserve the performance of inter-module communications, and the AXI bus is used for the connection between the baseband and application blocks.
- The baseband block is composed of the CTOP section including ARM11 for use in control and the WTOP section for use in signal processing.
- The GSM/GPRS and HSDPA sections are built into the baseband block and are controlled by it.
- The application block is divided into the L0 area run during standby and the L1 area that is used in normal operations.

Table General specifications of M2 and M1.

	M2	M1
Product name	μPD77620	MC-10038F1
Incorporated functions	Application/W-CDMA function, HSDPA (3.6Mbps) function (7.2Mbps possible using an external LSI), HSUPA co-processor IF, sound source function, GSM/GPRS function	Application/W-CDMA function, GSM/GPRS IF function
Circuit scales	Logic: 15M gate, ROM: 1.6M bits. SRAM: 12M bits (1p), 0.5M bits (2p)	Logic: 7M gate. SRAM: 8M bits (1 port). ROM: 0.5M bits.
Operating frequencies	Application block: ARM1176, DSP (500MHz operation) DBB block: ARM1156, DSP (250MHz operation) DDR I/F: 166MHz	Application block: ARM926, DSP (250MHz operation) DBB block: ARM926 (123MHz operation) DDR I/F: 125MHz
Process	65nm process Tr: LowVt/MiddleVt/HighVt mixed	90nm process Tr: LowVt/MiddleVt/HighVt mixed
Supply voltage	Internal: 1.2V ±0.1V I/O: 3.0V ±0.3V, 1.8V ±0.1V	Internal: 1.2V ±0.1V I/O: 3.0V ±0.3V, 1.8V ±0.1V
Package	FCBGA (PoP) 14 mm□,529-pin	0.5mm pitch FPBGA, 14mm□, 529-pin
Other	New technologies (LongRun 2, power SW) Memory redundancy Double cut via	Memory redundancy

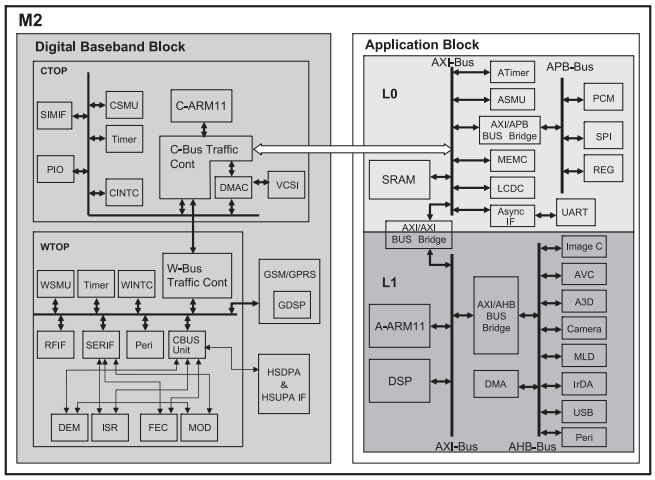

Fig. 1 Block diagram of M2.

5. Issues Regarding the Reduction of Power Consumption

The (SIMPULE N1) system mounting the previous M1 product featured a world leading operation time (700-hour continuous standby time (stationary) and 210-minute continuous talk time). The M1 contributed significantly to the achievement of these figures. It is intended that the M2 will continue to provide the low power consumption of the M1.

In general, power consumption consists of the dynamic power (power consumed by operations of the circuitry) and the leakage power (power consumed by leakage current). With the LSI for cellular phones, reducing the dynamic power can extend the communication time and reducing the leakage power can extend the standby time.

Now let us review the power design trend following the advancement of the miniaturization of the semiconductor process. If the scale and speed are constant, the dynamic power decreases due to semiconductor process miniaturization but the leakage power remains the same. However, as the advancement of a process by a generation increases the gate scale accommodated in the same chip size to 200% and the speed to 130%, the chip usually benefits from these advantages. As a result, both the dynamic power and leakage power of the new chip are approximately doubled (**Fig. 2**).

- Dynamic power: 1.8x = Gate scale 2x × Speed 1.3x × Dynamic power per gate 0.7x

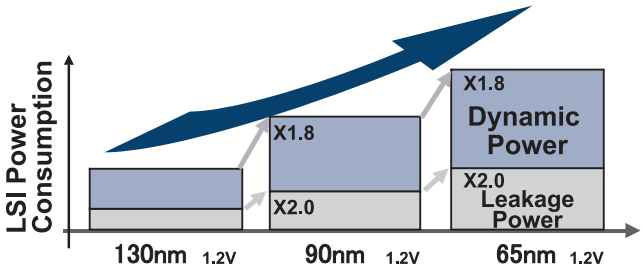

Fig. 2 Comparison of power (Increase in circuit scale and speed following the process generations).

- Leakage power 2.0x = Gate scale 2x × Leakage power per gate 1x

The above is precisely applicable to the relationship between the M2 and the previous M1. The addition of functions and improvements in performance for the M2 as shown in the above has almost doubled the circuit scale and we have decided to advance the process by a generation in order to package them in an equivalent chip size. As the performance requirement has been enhanced and the speed (operating frequencies) increased to around 130% to 200%, both the dynamic power and leakage power would be nearly doubled and the communication time would be decreased. In order to prevent this happening, we set the M2 design target to halve the leakage power and the dynamic power to achieve levels equivalent to those of the M1.

6. Power Consumption Reduction Technology Adopted

6.1 Reduction of Dynamic Power

We adopted the auto clock control technology as a means of extending the communication time by reducing the dynamic power requirement. Since the dynamic power is proportional to the signal operating ratio (frequency), it is usually reduced by stopping the clock in order to limit the operation at the minimum required level (clock gating) or reducing the frequency as required (dynamic frequency control). These control operations are generally executed based on specifications in the software, but it is difficult to create software that can always maintain the power at the minimum level, due to the necessity of optimization by manual input. We solved this problem by adopting automatic control based on the hardware. **Fig. 3** shows the clock circuitry of the function macros in the application CPU and other processing circuits.

1) An operation state monitoring circuit is provided for each function macro. When a low-load state is detected the system clock frequency is decreased automatically in order to reduce the dynamic power.

2) When one of the monitoring circuits detects an operation stoppage state, the power to the clock line is cut off. When the application CPU has stopped for a certain period of time, the power switch for the CPU (see below) is also switched off in order to reduce the leakage power.

3) The clock in each function macro is finely and hierarchically gated in order to reduce any unnecessary clock operations.

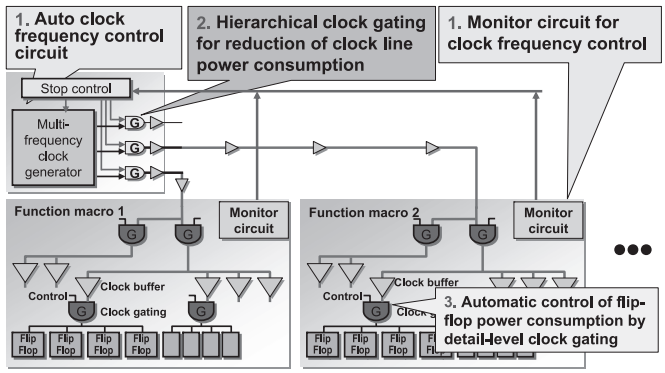

Fig. 3 Automatic clock control.

6.2 Reduction of Leakage Power

The standby time (period of the system standby mode) is determined mainly by the leakage power (power consumed by the leakage current when the handset is not operating). To reduce the power consumption and extend the standby time of the M2, we incorporated three kinds of transistors and a power switch for use in cutting off the leakage power in the standby mode.

The following three kinds of transistors with different Vt (threshold voltages) are used according to the degree of compatibility between high-speed operation and low leakage power.

1) HighVt

The speed is low but the leakage power is small. These transistors are used mainly in the digital baseband circuit that is always ON.

2) MiddleVt

The speed is 1.5 times higher than for the HighVt transistors but the leakage power is higher by more than 10 times. These transistors are used in those parts of the circuits where the speed of the HighVt transistors is inadequate.

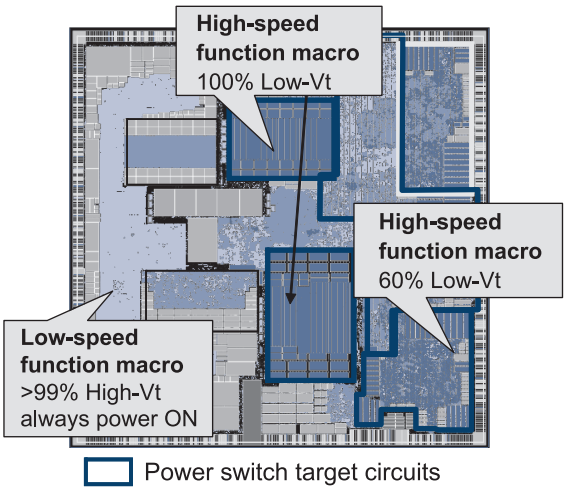

Fig. 4 Examples of applications of transistors.

3) LowVt

The speed is twice that of the HighVt transistors and the leakage power is higher by more than 100 times. These transistors are used in the application CPU and DSP, which need 500MHz operations.

The circuits incorporating the LowVt transistors have leakage power from a few to tens of milliwatts. They should therefore be turned off in the standby mode. In order to reduce the leakage power of the M2, we incorporated power switches in seven circuits using LowVt transistors to switch the individual circuit OFF when not in use. The power switches enable finer power control than is possible by switching the LSI ON-OFF by external means. The application CPU of the M2 is switched OFF when the OS is in standby mode and can be started up in a few microseconds after receiving the interrupt signal. An easy-to-use power saving function based on software has thus been implemented (**Fig. 4**).

6.3 Power Consumption Reduction Effect

We succeeded in controlling the power consumption of the M2 at a level equivalent to that of the M1 by making full use of the power consumption reduction technology described above.

Fig. 5 shows the results of the evaluation obtained by running an actual music reproduction application. The application required only light processing and belonged to the kind of application for which the largest power saving effects can be expected when run on a CPU of 500MHz operation frequency. We succeeded in reducing the power consumption to 1/5th thanks to the auto clock control and power switch control.

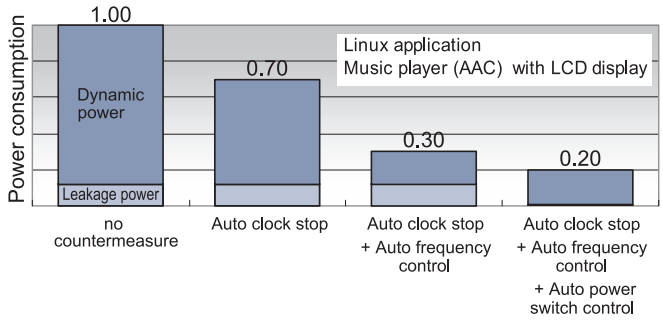

Fig. 5 Effects of auto clock control and power switches.

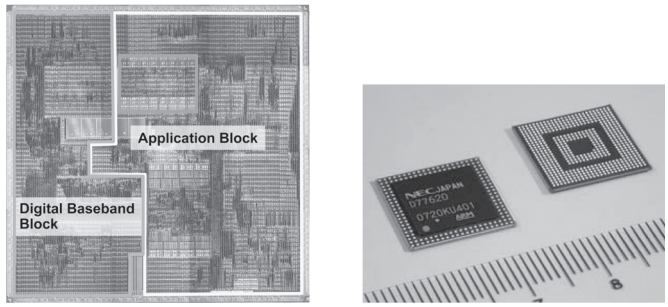

Photo M2 chip and product appearance.

7. Achievements of the M2

NEC Electronics was able to package the M2 in a chip size of 9.52 × 8.52 mm ^{2} in spite of the large circuit scale integrating both the application and baseband blocks. The package used was a 529-pin PoP with a universal memory chip mounting capability as was initially planned. **Photo** shows the chip and an external view of the product.

In addition, from considerations of the mass-production process, we applied memory redundancy and double cut via and their percentages of applicability are respectively 60% (approx. 7M bits) and 55%. This strategy has made it possible to ensure the required mass-reproducibility.

The M2 can be used to achieve standby and communication times at the world's highest levels and equivalent to those of the previous M1.

8. Conclusion

Using the most advanced 65nm process, the M2 contributes to improvements in the performances of mobile handsets

by achieving a power performance comparable to that of the previous M1 even though its market share has more than doubled. This has been achieved by making full use of power consumption reduction technologies. As the requirements related to the functions and performances of applications and communications are expected to advance in the future, we are continuing to develop and market LSIs by pursuing power consumption reductions suitable for mobile handsets and by incorporating new technologies for the further satisfaction of our customers.

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