EMMA3, an LSI for HD DVD Player/Recorder Systems

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Abstract

NEC Electronics released a world first system LSI that is compatible with both HD DVD players and recorders. This LSI processes the digital video, audio and graphics required for the HD DVD player. By the compatibility with the current video and audio compression standards including “MPEG-4 AVC/H.264” and “VC-1” that have been adopted to support the next-generation DVD, it is able to deal with advanced applications. The device is equipped with a stream processing capability and with multi-channel stream input/output for use in the recording of digital broadcasts. Any system that incorporates it may easily be extended in order to function as an HD DVD recorder.

Keywords

HD-DVD, player, recorder, system LSI, digital broadcasting, digital HDTV broadcasting, MPEG-4 AVC/H.264.VC-1

1. Introduction

The recent expansion in the coverage of digital HDTV broadcasting by the use of BS and the Air digital broadcasting techniques has been rapidly promoting the incorporation of digital HDTV compatibility among TV receivers. Moreover, as users have begun to seek out high-quality video as a disc media of choice, HD DVD as the next-generation DVD is providing compatibility with the same digital HDTV quality that was previously available with digital broadcasting. At the same time as the improvement in video quality, more and more video content began to appear as interactive features in the disc media. As the prices of the players for such products are rapidly shifting toward the popular area in the widely acceptable price zone, it has become urgent to develop a system LSI that enables a reduction in the system cost at the same time as increasing the range of its functions.

In order to meet such market trends, NEC Electronics has released a world-first HD DVD player/recorder LSI, “EMMA ™ 3” that incorporates HD DVD playback and a digital HDTV broadcasting reception capability (**Photo 1** , **Fig. 1**)

2. Features of EMMA3

The main features of EMMA3 are as follows.

1) Simultaneous HD/SD Decoding

Simultaneous HD+SD decoding of the format required for an HD DVD player including MPEG-4 AVC/H.264, VC-1 and MPEG2 MP@HL is possible.

In addition, the simultaneous reception/recording of two digital HDTV broadcast programs is also possible with a single chip. This is an essential feature for a digital HDTV recorder.

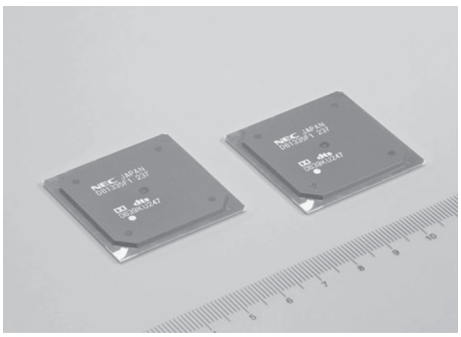

Photo 1 EMMA3 (μPD61335).

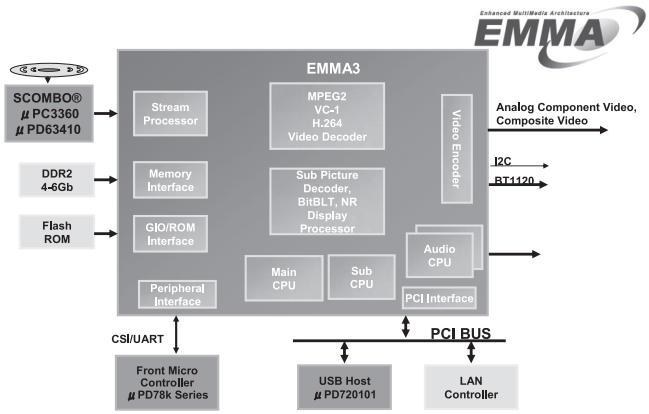

Fig. 1 EMMA3 block diagram.

2) High-Performance Stream Processor
Its flexible and high-speed stream processing function can deal with HD DVD sources and digital broadcasting. This capability enables the hybrid playback of an interactive story of HD DVD using the Internet.

3) 2-CPU Architecture
EMMA3 features main and sub CPUs that are used by the applications and drivers. The sub CPU controls the real-time processing of the drivers, a function that is close to that of hardware while the main CPU has the facility to process interactive user applications. The allotment of functions between the two CPUs facilitates systems development by users.

3. Outline of EMMA3 Functions

3.1 CPUs

The main CPU is the VR5500, which is an NEC Electronics original 64-bit RISC CPU. This is a high-performance CPU incorporating a 64K-byte instruction cache and a data cache for the flexible handling of applications.

The sub CPU is a 32-bit RISC CPU manufactured by MIPS Technologies that has an 8K-byte instruction cache and a data cache for use by the driver and for AV processing, which needs a real-time property.

3.2 Stream Processor

This is an NEC Electronics original processor dedicated for stream processing. In addition to various streams including DVD-Video, DVD-Video Recording and ARIB digital broadcasting, it is also capable of dealing flexibly with the HD DVD standards.

3.3 Video Decoder Engine

The video decoder engine is compliant with the MPEG-4 AVC/H.264, VC-1 as well as with the MPEG2 MP@HL and MPEG1. Its compatibility with dual decoding of MPEG2 MP@HL allows it to execute SD downconversion/decoding, which is used to decode/re-encode and convert a program into the DVD-Video recording format at the same time as performing digital broadcasting reception.

3.4 Audio Decoder Engine

The audio decoder engine incorporates two 32-bit RISC CPUs. It is compatible with the simultaneous playback of audio formats including Dolby Digital Plus, True HD and the DTS-HD, and also the effect-processed audio.

3.5 Unified Memory Architecture

Unified memory architecture is supported in order to allocate continuous address spaces to two DDR2 SDRAM interfaces and to process the entire data transfer request from all of the units that use memories. The DDR2 SDRAM interfaces allow independent access to the two bus systems including 655. 36MHz 32-bit and 16-bit buses. The connection of memories of up to 8192M bits is also possible.

3.6 DMA Controller

DMA transfer between internal units of the TS input/demultiplexer, MPEG decoder engine and/or audio decoder engine and the DDR2S SDRAMs and high-speed DMA transfer between DDR2 SDRAMs are possible as well as the automatic execution of multiple DMAs without the intervention of the CPUs. This reduces the CPU load in copying and transferring segmented data.

3.7 Extension Memory Interface

Connection of NOR and NAND type flash memories are supported and up to four chip select signals and a 64M-byte area are supported as an external ROM interface. As a universal I/O interface, up to four chip select signals and a 16M-byte area per chip select signal are also supported.

3.8 ATA/ATAPI Interfaces

Two industry-standard parallel ATA interface channels are built in to support the PIO mode and Ultra-DMA100. Up to four drives can be handed by connecting an HDD and optical drive to the master and slave of each channel.

3.9 Display Controller/BitBLT Engine

A powerful display controller engine is incorporated to deal with the next-generation DVD.

The main display supports two HD-sized video planes, four

OSD planes and a back color. It is compatible with the anti-flicker filter, 256-level alpha blending, motion adaptive IP conversion for SD and various noise reduction procedures.

The sub display corresponds to the traditional analog TV and supports one SD-size video plane and one OSD plane. In addition to a recorder it features a digital output that can be used in channel downconversion (scaling) recording.

The OSD supports 2-, 4- and 8-bit/pixel color lookup table formats as well as RGB32 and RGB16. It is also compatible with transmission processing using α (alpha)-blending.

The BitBLT engine supports a high-speed 2D image block transfer function, a color space conversion function that is effective for font deployment and a size conversion function, etc.

3.10 External Video/Audio Input/Output

The supported external inputs are a digital video interface of the ITU-R Bt.656 format and a PCM audio input.

The supported two external video output are ITU-R BT. 1120/BT.656 compliant digital for the output of digital signals such as HDMI. The audio outputs are the PCM data output and the stream data output from the S/PDIF.

Table EMMA3 specifications.

Video decoder	·MPEG2 video MP@HL, MP@ML standard, MPEG1 video standard ·MPEG4 AVC/H.264 HP@L4.1, MP@L4.1, L3.2 ·VC1 AP@L3, AP@L2, full trick play, JPEG decode accelerator ·MPEG4 ASP@L5 visual standard without 1/4 pixel, global motion compensation
Audio decoder	·Dolby™ Digital, Dolby Digital Plus, Dolby True HD, DTS™, DTS-HD ·MPEG1 Layer 1/2, MPEG2 AAC, MLP, LPCM for DVD, CD-DA, MP3, WMA
Stream processor	·Based on HD DVD, DVD-Video, DVD-Video Recording, DVD+VR, Video CD 2.0, ·ARIB, MPEG2-TS, MPEG2-PS and MPEG1
Scramble functions	·CSS descrambler, CPRM, AACS scrambler / descrambler ·DES, 3-DES, AES encryption / decryption engine ·Multi-2 ARIB
Main CPU	·64/32-bit RISC, 655 Dhrystone MIPS at 327 MHz frequency
Sub CPU	·32-bit MIPS32™ CPU Core, 457 Dhrystone MIPS at 327 MHz frequency
Storage interface	·Two parallel ATA / ATAPi interfaces, Ultra-ATA100
Video encoder	·NTSC / PAL / SECAM / HDTV (720p / 1080i / 480p / 576p) ·simultaneous YPbPr, Y/C analog output
Digital video output	·ITU-R BT. 656, 1120
Digital audio output	·IEC61937
Peripherals	·I2C, clocked serial interface, UART, timer
PCI	·3.3V 32-bit PCI at 33MHz
Unified memory	·32/48-bit bus width, DDR2-667 SDRAM
ROM interface	·NOR / NAND Flash ROM
Power supply	·1.0V, 1.8V and 3.3V

3.11 Video Encoder

The video encoder can encode the main video of the digital video output and the re-encoding output as well as the main video and sub video of the analog video outputs. The analog main video output can output YPbPr/YCbCr signals from the 148MHz 10-bit DAC. The sub video output can output a composite video or Y/C video signal from the 54MHz 10-bit DAC.

3.12 Peripheral Functions

Almost all of the peripheral device interfaces required to support a DVD player/recorder have been built in. These include a 33MHz, 32-bit PCI.2.2-compliant PCI bus interface, three UART interfaces, three I2C interfaces, three CSI interfaces, one Smart Card interface and one IR transmitter interface.

Table shows the specifications of EMMA3.

4. Software Architecture

Fig. 2 shows a typical example of the software configuration of the EMMA3. Hardware control that needs real time control executes on the RTOS in the sub CPU, while the user application executes on Linux in the main CPU. The information communication between the CPUs is executed by the inter-CPU communication driver. This configuration contributes to the differentiation of the sets incorporating EMMA3 and features a clear division of work between the CPUs, thereby

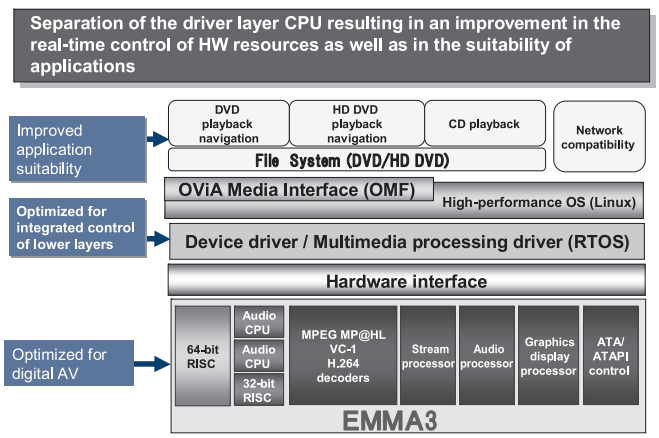

Fig. 2 EMMA3 software configuration.

allowing users to dedicate themselves to application development.

The software that we offer is driver software at and below the inter-CPU communication driver level that features common interfaces to enable users to have direct awareness of the hardware.

Such software interfaces may be adopted as standard by the EMMA range of LSIs in the future and thus enable a diverted use of software assets. The main CPU uses industry-standard Linux as the OS in order to contribute to an improvement in the software development efficiencies of users by reducing the development term.

5. Development Environment

Photo 2 shows the evaluation board of the EMMA3. This board accepts the connections required by the player/recorder such as the disk drive and stream input connections, so that various evaluation and development operations are possible using the driver software that we provide.

6. Conclusion

This paper has described the features of EMMA3. The use of this LSI enables construction of an HD DVD player and recorder on a common platform. The recorder thus implemented offers advanced functions at low cost, such as 2-program simultaneous recording and one of the programs may be played back during recording.

We plan to continue active development of such devices and to release a series of LSIs designed to support the next-generation DVD player/recorder systems as well as associated equipment in support of a market that is expected to expand in the future.

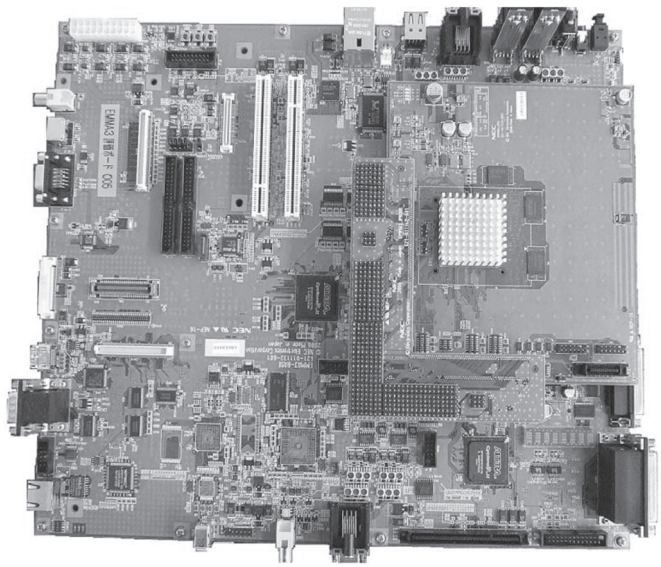

Photo 2 EMMA3 evaluation board.

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