SMAFTI Package Technology Features Wide-Band and Large-Capacity Memory

KURITA Yoichiro, SOEJIMA Koji, KAWANO Masaya

Abstract

NEC Electronics Corporation and NEC Corporation have jointly developed an ultra-compact system-in-package (SiP) that connects the memory chip and logic LSI through a high-density wiring body. This technology features co-existence of the wide-band memory accessibility of the system-on-chip (SoC) and a memory capacity increase capability of the SiP that is made possible by the individual fabrication of memory and logic on independent chips. This package is expected to improve performance due to memory band widening and a reduction in the power consumed in inter-chip communications. Practical implementation is being advanced by aiming at a broad field applications field including the mobile equipment market, which is currently undergoing a rapid multiplication of functions.

Keywords

System-in-Package (SiP), interposer, wiring technology, connection technology

1. Introduction

The evolution of information processing and communications technology and the spread of the Internet have promoted the ubiquity of advanced digital information equipment that may be used in any location, from cellular phones to supercomputers. As well as the traditional requirements associated with the evolution of technology such as improvements in functions and an increase in speed, these new types of information equipment are subject to additional requirements that are regarded as critical. These include a reduction of power consumption per performance and size constraints. With the IC chips that form the core of the digital information processing systems, the increase in the processing speed and memory capacity is significant due to the decrease in device sizes. However, performance improvements are beginning to tail off in contrast to the increase in the development and fabrication costs of device micro-fabrication.

On the other hand, performances have come to be determined often by the capability of data transfer between the processors that compute information and the memory that stores data. This is particularly so with high end information processing systems such as mobile information and image processing equipment and supercomputers. As a result, with these applications, it has become essential to improve the memory bus capability, in order to achieve a coexistence of high performance and low power consumption. The system-on-chip (SoC), which forms the logic and memory circuits required for such a system on a single chip, can deal with this requirement by reserving a sufficient bandwidth with low power consumption due to its on-chip wiring. However, with the current silicone LSI chips, the device structures and fabrication processes are completely different between the logic circuit that computes and controls information and the memory circuit that stores the processed data. In particular the DRAM is used universally as the work memory/main memory and this makes it hard to fabricate an SoC with a large-capacity memory at low cost due to the tradeoff between the cost and memory capacity. Meanwhile, the system-in-package (SiP) has recently been put to practical use, particularly for mobile equipment. The SiP is fabricated by arranging the logic LSI and memory as independent chips and connecting them using the wire bonding technology, etc. This structure makes it possible to fabricate the logic LSI and memory independently, using the respectively optimized device configurations and wafer processes. However, its bus width, the electrical characteristics of the transfer path and power consumption of the I/O are much inferior to the SoC because the chips are interconnected electrically either by means of wire bonding or the package substrate.

A solution for this problem is the Chip-On-Chip (COC) structure, which installs the logic LSI and memory circuits so that their circuit sides are opposed to each other and to connect them through the electrode terminals (bumps) and install them as an area array. The COC structure makes it possible to in-

crease the bus width because the chips are interconnected through electrodes installed in an area array format. It can also improve the electrical characteristics such as to reduce inductance due to the exclusive use of the bumps for inter-chip transfer and reduce the power consumption thanks to a reduction in the load to the I/O circuits of both chips. However, there have also been certain restrictions with the COC package connecting the logic LSI and memory, e.g., memory capacity limitations, depending on the chip size and the limitation of the means of connecting the logic LSI to external terminals by wire bonding only. To solve these problems, we have recently developed a general-purpose LSI package[1] that connects a large-capacity memory to a logic LSI via a wide bus of some hundreds of bits, and named it the SMAFTI (SMArt chip connection with Feed-Through Interposer).

2. Configuration of the New Package

Fig. 1 shows the concept and structure of the newly developed SiP. The overall structure is composed of the logic chip, memory chip and fine wiring called the FTI (Feed-Through Interposer), which is inserted between them. The FTI is an interposer on which fine wiring patterns are formed and are supported by the molded resin that also seals the memory chip. On the logic chip, a BGA (Ball-Grid Array) is formed for use as the external electrode terminals. The FTI is composed of a polyimide insulating resin layer and conductor wiring pattern, and the insulating resin layer has a conductor passing through it. For the interconnection between the logic LSI and memory chips, the electrode bumps of the memory chip are connected to the conductor pad on the upper side of the FTL and are connected to the electrode bumps of the logic LSI chip via a conductor located immediately below the pad. The inter-chip connection section can be installed in the form of an array with a pitch below 50μm which makes it possible to interconnect logic and memory chips over 1000 bits. The external electrode terminals of the logic LSI chip are placed on the chip periphery so that they surround the inter-chip connection section, and connect to the BGA via the conductor and wiring of the FTI. The FTI wire pitch can be fabricated as small as about 10μm.

Interconnecting the chips and leading the external terminals of the logic LSI through an FTI with a high-density conductor

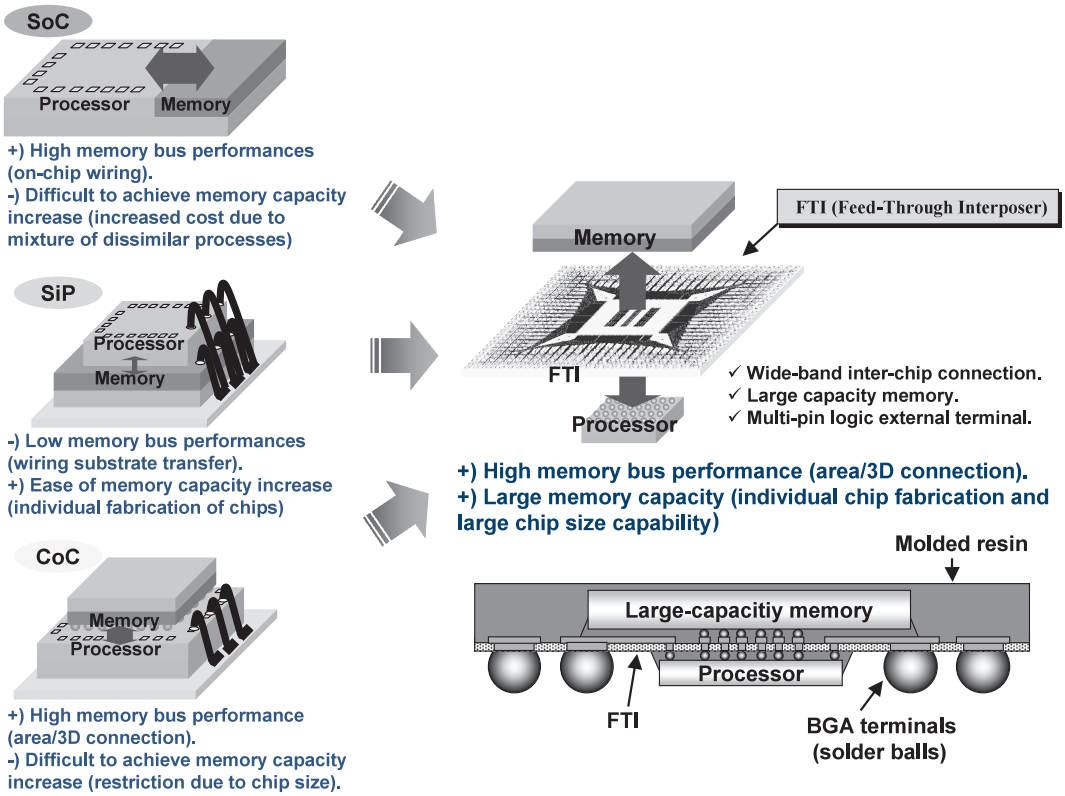

Fig. 1 Concept and structure of the SMAFTI package.

and wiring pattern makes high-density inter-chip connections possible and multiplication of the logic LSI's external terminals. Due to the freedom from chip size restriction that accompanies the traditional COC package structure, it is also possible to mount a large-capacity memory on the package.

3. Fabrication Process

One of the most significant features of this package is that it is fabricated completely in the wafer stage. We have recently fabricated a package prototype using TEG chips based on the specifications shown in **Table 1**. TEG chips are designed so that the inter-chip connections become daisy chain connections when they are packaged and the opening/grounding of the inter-chip electrical connections can be confirmed via the logic TEG chip – FTI wiring – BGA terminals.

Fig. 2 shows the flow of the fabrication process. First, a Si wafer is used as the support body and each wiring body (FTI) is formed using Cu wiring and a polyimide insulating film on the Si wafer. Then, the memory TEG chip on which SnAg solder-plated bumps are formed is bonded onto the FTI using flip chip bonder, and the bonded area is sealed with under-fill resin. The bonding is performed by a flux-less local reflow process in a nitrogen atmosphere. Since the wiring body is formed on the Si wafer, there is little risk accompanying the flip chip connection of ordinary organic resin substrates being caused due to differences in the linear expansion coefficients, such as the degradation of connection accuracy or destruction of the connection section by residual stress. This allows the chip to be connected with a narrow pitch of 50μm or less as seen with the present sample.

Photo 1 shows the external view of the wafer with the wiring body formed and the chip bonded onto it. Next, the surface of the wafer with bonded chip is sealed with a compressed molding process, and the supporting Si wafer is removed to expose the wiring pattern of the FTI. When a resin wafer with an embedded memory TEG chip is fabricated as described above, a logic TEG chip on which solder-plated bumps are formed in the same way as for the memory TEG chip is bonded with a local re-flow process and the bonding section is also sealed

Table 1 SMAFTI package – prototype specifications.

Item	Specifications
Logic TEG chip size	5.31 × 5.31 mm
Memory TEG chip size	7.35 × 12.7 mm
Inter-chip connection	50μm (area array)
	400-pin
Logic TEG external electrode	35 μm staggered (peripheral)
	500-pin
Package appearance	Fine-pitch BGA
Package size	15 × 15 mm
BGA terminal	0.5 mm pitch
	500-pin

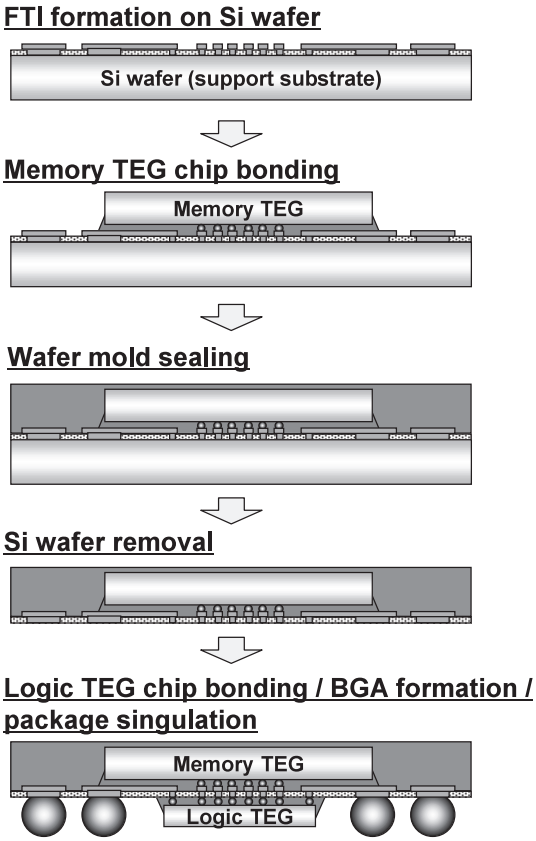

Fig. 2 SMAFTI package fabrication flow.

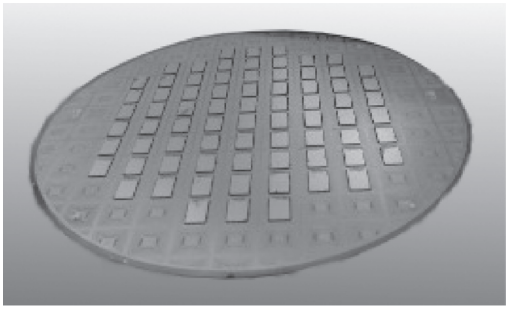

Photo 1 chips bonded onto FIT forming wafers.

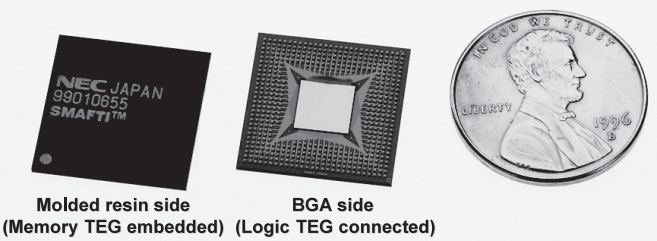

Photo 2 Chips bonded onto FTI forming wafers.

with under-fill resin. In this case, too, high bonding accuracy and quality can be ensured because of the connection between the Si of the thick memory chips by means of the very thin FTI. Finally, SnAgCu solder balls are bonded onto the pad formed on the FTI on the resin wafer, and each package is separated by dicing.

Photo 2 shows the external view of the completed package, **Photo 3** shows a cross-sectional SEM micrograph of the entire package, and **Photo 4** shows a cross-sectional photo of the 50μm pitch inter-chip connection through the FTI. This photo allows us to confirm that the optimum structure is realized including the inter-chip connection via the conductor channel of the FTI and the connection from the logic TEG chip to the BGA terminals also through the FTI.

As described above, the SMAFTI features the very unique fabrication process of interposing the wiring body formed on Si wafer by repeating its transfer to the Si chip. This process has enabled high-density inter-chip connection by means of bonding with matched coefficients of linear thermal expansion between the Si through a fine wiring body. In addition, the fact that the fabrication process is performed consistently in the wafer state from the formation of the interposer to the assembly is expected to improve the productivity thanks to the integrated handling mode and to also improve the plant investment efficiency thanks to the possibility of transferring or utilizing the existing production facilities for wafer level packages, etc.

4. Evaluation of Inter-Chip Connection Reliability

We conducted the primary stage of the reliability evaluation of the most significant feature of this technology, which is the inter-chip connection through the FTI. We first evaluated the under fill resin that is regarded significantly affecting reliability by performing temperature cycle testing on samples made by using two kinds of resins with different mechanical properties. **Table 2** shows the mechanical properties of the evaluated under fill resins, **Table 3** shows the pre-processing and temperature cycle processing conditions used in the evaluation, and **Table 4** shows the results of the connection reliability

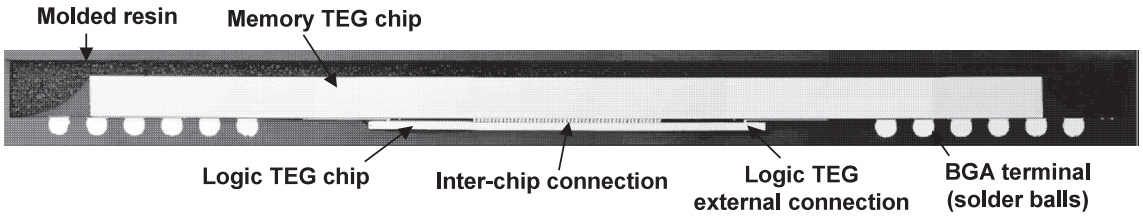

Photo 3 Cross-section of SMAFTI package.

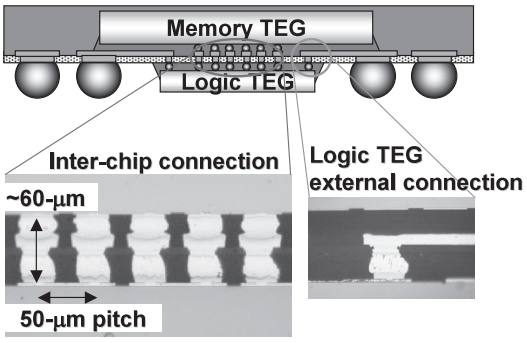

Photo 4 Cross-section of micro-bump through the FTI.

Table 2 Mechanical properties of the under-fill resin.

Resin Properties		Resin A	Resin B
Tg (℃)		120	150
Coefficient of linear thermal expansion(ppm/K)	<Tg	40	30
	>Tg	130	90

Table 3 Test conditions.

Processing Item	Conditions
Pre-treatment	Thermal Cycle: -55～125℃ / 20 cyc Prebake: 125℃ / 10 h Moisture Absorption: 30℃, 70%RH / 168 h IR Reflow: Max 260℃ / 3 times
Temperature cycle test	-55～125 (10 min / 10 min)

Table 4 Temperature cycle test results.

	0 Cyc *	100 Cyc	300 Cyc	500 Cyc	1000 Cyc
Resin A	2/5 Fail	1/3 Fail	0/2 Fail	2/2 Fail	---
Resin B	0/5 Fail	0/5 Fail	0/5 Fail	0/5 Fail	0/5 Fail

*Measured after pre-treatment

testing. We made right/wrong judgments by checking the electrical conductivity of the daisy chain of the inter-chip connection after pre-processing and after each temperature cycle processing. Although the temperatures used in the temperature cycle testing were below the glass transfer temperatures (Tg) of the resins, failures of connection opening were observed with resin A with a relatively higher coefficient of linear thermal expansion (CTE) as early as after pre-processing. On the other hand, with resin B with a relatively low coefficient of linear thermal expansion, no failure was observed even after 1,000 cycles. Since the connection in question is performed between Si chips, it is regarded as being hardly affected by the horizontal stress due to the differences in the coefficients of linear thermal expansion of the substrate and the Si chip, which may occur with an ordinary flip chip connection using an organic resin substrate. As a result, we estimated that the opening failure was caused when the stress due to the mainly vertical thermal expansion/compression of the under-fill resin destroyed the bonded section. We are planning more detailed analyses, optimization of the bonding conditions and resin properties and other, more advanced reliability evaluations in the future.

5. Conclusion

We propose a general-purpose package “SMAFTI” that can connect devices such as logic and memory chips using a wide bus of 1,000 bits or more. We have actually prototyped such a package using TEG chips and have confirmed the applicability of the structure and fabrication process as well as the basic reliability of the connection method. In the future, we propose to continue development by aiming at establishing this system as a universal technology that can be applied to a wide range of applications.

Reference

1) Kurita, Yoichiro, Soejima, Koji, Kikuchi, Katsumi, Takahashi, Masatake, Tago, Masamoto, Koike, Masahiro, Shibuya, Koujirou, Yamamichi, Shintaro, and Kawano, Masaya: “A Novel ‘SMAFTI’ Package for Inter-Chip Wide-Band Data Transfer,” Proc. of 56th Electric Components and Technology Conference (ECTC 2006), pp. 289-297, 2006.

Authors' Profiles

KURITA Yoichiro
Assistant Manager,
Advanced Device Development Division,
NEC Electronics Corporation

SOEJIMA Koji
Assistant Manager,
Advanced Device Development Division,
NEC Electronics Corporation

KAWANO Masaya
Team Manager,
Advanced Device Development Division,
NEC Electronics Corporation