Failure Analysis Technology for Advanced Devices

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Abstract

The sophistication of functions, miniaturization and reduced weight of household appliances and various devices have been accelerating in recent years. The LSIs loaded into these products have consequently been significantly miniaturized into microscopic sizes on an increasingly large scale. In the midst of all this, a failure analysis technology is an extremely critical technology used in situations that call for identifying design problems with short delivery designs, the clarification and resolution of problems in manufacturing processes, as well as the resolution and feedback of problems within a short time in the unlikely event of problems occurring at a customer's location.

This paper introduces technologies along with case examples, such as fault diagnosis for accurately narrowing down the locations of faults, fault localization that pin points the determination of such locations and a physical analysis important for clarifying problems efficiently and in a short period of time.

Keywords

LSI, IC, semiconductor, logical circuit, failure, defect, analysis diagnosis, physical analysis, analysis, fault localization, cause of failure

1. Introduction

It is extremely important to diagnose faults, localize faults and physically analyze, in a coordinated manner, to clarify the faults of LSIs that are being increasingly miniaturized into micro sizes and increasing in scale, to raise the level of their sophisticated functions efficiently and in a short period of time (**Fig. 1**). Fault diagnosis is a technology used for making logical estimations of fault locations based on the internal operations of circuits using design data and inspection results. The narrowing down of candidates for faults is performed automatically to gate levels and the results are output. Based on the information obtained, the fault locations are identified using various failure analysis equipments, such as emission microscopes or OBIRCH equipment, pin pointing their location. Furthermore, a physical analysis clarifies the physical causes with measurements of transistor characteristics taken at locations where faults are caused, while cross sections are observed with scanning electron microscopes (SEM) or transmission electron microscopes (TEM), as well as through various other means and devices including an elemental analysis. The technologies are introduced next.

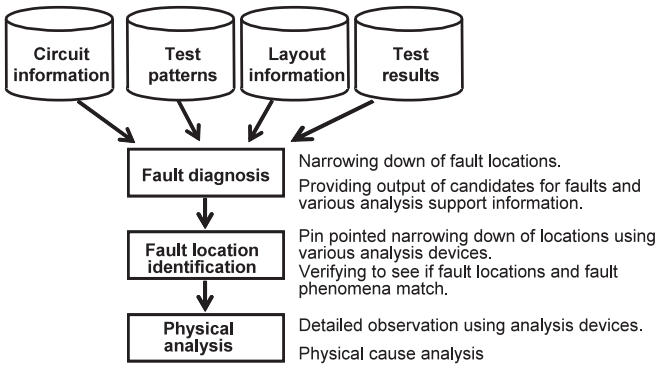

Fig. 1 Failure analysis flow.

2. Fault Diagnosis Technology

The fault diagnosis system uses circuit information, test data for inspections and inspection results to make a diagnosis. A diagnostic method[1] of a path tracing type, a proprietary development of NEC Electronics, is used for the diagnosis algorithm of the system. Unlike the fault dictionary method or fault simulation method that use the assumptions of fault models prepared in advance, this method estimates the failure location by tracking the input direction of error propagation paths based on the failure output from the results of tests on the LSI. Furthermore, the method categorizes[2] the failure modes of stuck-at 0/1, open and bridge type

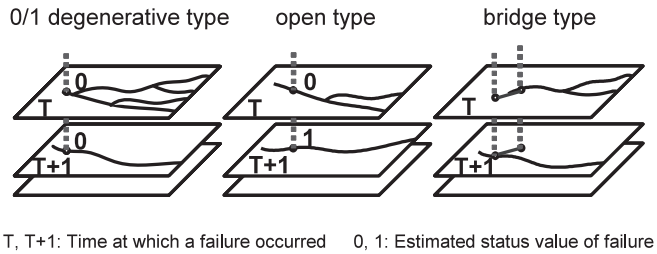

Fig. 2 Categories of failure modes.

faults, based on the inferred values of candidates for faults as shown in **Fig. 2**.

T and T+1 in the figure represent the times at which failures occur. Error propagation paths and their inferred values are shown. Stuck-at type fault is a mode in which the logic value is constantly fixed to 0 or 1, while open fault type is an unstable mode with the logic values varying in the time frames in which the failures occur. Bridge type fault is a mode that has opposite expected logic values in the time frames in which failure at outputs are observed.

Furthermore, the wiring distribution information of the layout, as well as error propagation paths are used to narrow them down with more detail. Layout coordinate information effective for identifying fault locations can also be output, increasing the efficiency of the actual analysis.

This algorithm can also be extended to deal with delay faults and multiple faults, making it possible to diagnose even when faults are simultaneously occurring at multiple locations. This is due to the fact that problems relating to variations arising from microscopic processing are expected to frequently manifest as delayed failures, and since problems arise due to manufacturing equipment among problems relating to manufacturing. The problems of causing manufacturing are unlike design problems or running trouble in the passing of time, and failures are found simultaneously at multiple locations. The candidates for multiple faults are output accurately by improving the algorithm for tracking the error propagation paths and grouping those paths[3,4].

The ratio of the number of candidates for faults, derived from the results of a diagnosis actually conducted recently, is shown in **Fig. 3**. The figure indicates that a little under 80% of the total number could be diagnosed automatically with this fault diagnosis system. Of the findings, it is clear that over 65% of all single incident and multiple incident failures combined can be attributed to the candidates whose numbers can be narrowed down to five or less.

A case example for which an analysis was made based on the diagnosis results is introduced in Section 3.

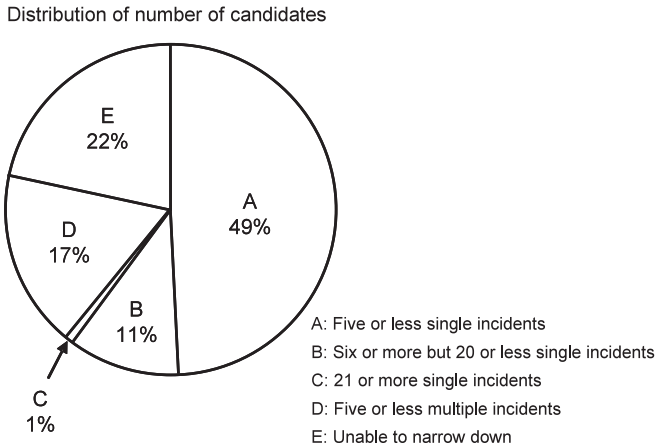

Fig. 3 Ratio of diagnosis results in terms of number of candidates for faults.

3. Fault Localization Technology

In this section, our failure analysis method with the SDL (Soft Defect Localization) at NEC Electronics is presented, that uses the results of fault diagnosis covered in Section 2. The method is important for localizing marginal failures, such as timing failures. SDL[5] is a fault localization technique proposed for marginally defective devices, that fail in tests depending on the power supply voltage and timing conditions even within the ranges of voltage and timing conditions specified for the products. An example of the Shmoo plotting for a marginally defective device is shown in **Fig. 4**.

The SDL analysis is performed with the OBIRCH equipment[6] linked with an ATE, as shown in **Fig. 5**. The operation of the SDL involves repetitive application of a short test pattern with the power supply voltage and timing condition around the pass/fail borderline on the Shmoo plotting. While this is being performed, a rectangular area of the device is exposed to a slowly scanning laser beam (with a wavelength of 1,300nm) from front side or back side. In this process, the scanning speed is made adequately slow to ensure that a pass/fail is determined by one test pattern cycle at each point of the laser scan. When a device is exposed to the laser beam in this manner, the pass/fail states of the defective location may vary due to the effect of the added heat, which can change the resistance value at a high-resistance fault, a bridge fault, or other fault in the device. An SDL image is generated when the mapped pass/fail results obtained in this manner are displayed in black and white.

At NEC Electronics, we are applying the SDL technique in the procedure shown in **Fig. 6**. SDL reactions are less likely to be

Fig. 4 Example of Shmoo plotting (horizontal axis represents power supply voltage, while vertical axis represents test rates. The lower the coordinate the faster the operating speed. The red color marks the borderline between pass and fail.)

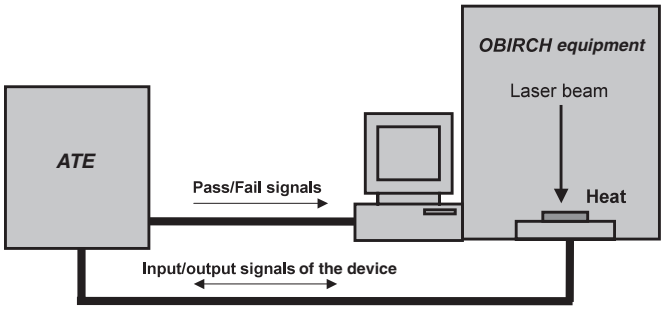

Fig. 5 System configuration of SDL.

detected when wide angle lenses with lower magnification are used, while the detection tends to be made easier when higher magnification lenses are used. For this reason, analysis efficiency can be increased by first performing the fault diagnosis in Step 1, to narrow down the candidate locations in advance, as shown in the example of **Fig. 7**, then taking SDL measurements to the predetermined range using lenses with higher magnification. A test program for repeating tests on devices in a short period using conditions around the pass/fail borderline and providing pass/fail results is arranged in Step 3. In Step 4, the silicon chip is heated and the pass/fail state changes are confirmed in advance.

An SDL image similar to **Photo 1** can be obtained by performing SDL measurements according to the procedure described above. An example of a defect is shown in **Photo 2**, which are detected by a cross sectional observation around the reaction site.

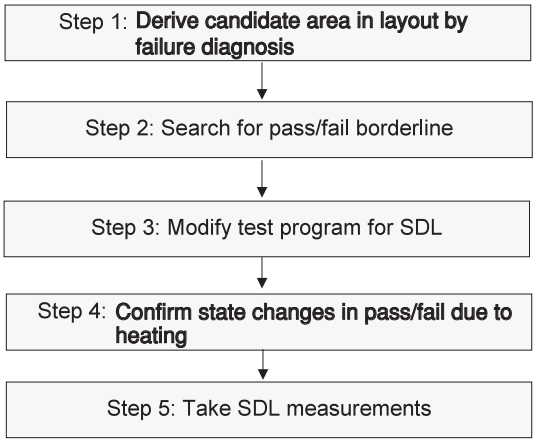

Fig. 6 Procedure for SDL analysis.

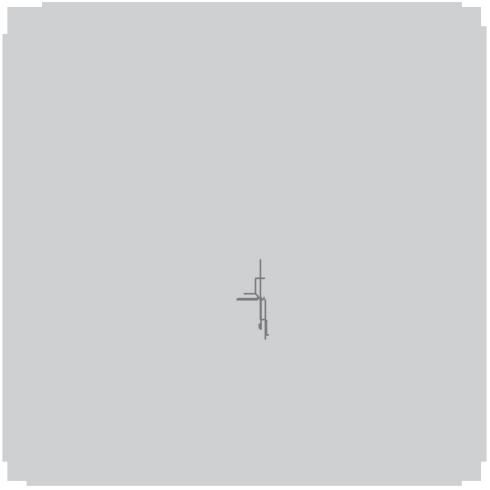

Fig. 7 Example of range for candidates by failure diagnosis plotted on chip layout.

4. Physical Analysis Technology

Analysis technologies effective primarily for detecting high-resistance defects and short circuit defects, in places such as wiring locations or via holes, have been introduced thus far. When characteristic defects exist in transistor (Tr) segments, it is necessary to take direct measurements of the arbitrary transistor characteristics and analyze multiple aspects. In the past direct measurements of characteristics for arbitrary transistors in an LSI had been difficult. The cause of the defects were extremely difficult to clarify because transistor defects could have been caused by the shape of the transistors or they could have been triggered by minute

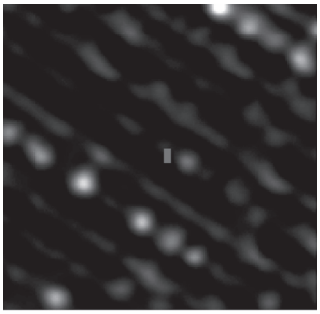

Photo 1 Example of SDL image overlaid on a pattern image. The small rectangle region in the center represents pass, while other region represents fail.

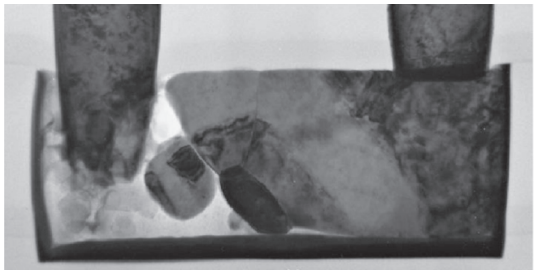

Photo 2 Example of detect observed by cross-sectional observation at the SDL spot.

abnormalities in the amount of dopants used. The technology implemented recently for taking direct measurements of various individual transistor characteristics, as well as examples of a physical analysis for transistor defects, are introduced in this section.

A device called a nanoprobe, located inside the SEM device, has been developed to take measurements of arbitrary transistors in LSIs by manipulating a number of needles with extremely sharp points to directly probe contact plugs inside LSIs. This probe is in practical use in the field for failure analysis. LSIs are polished evenly as shown in **Photo 3** and probed while the location is observed with the SEM device, with direct measurements taken of individual transistor characteristics. This technology is a useful technology for investigating abnormalities among multiple transistors, which are candidates for faults. Through the implementation of this technology it has become possible to analyze failures with SRAM memories almost completely.

The result of the measurements taken using this nanoprobe device for the analysis of defective transistors inside an actual SRAM, is shown in **Fig. 8**. A transistor that indicates abnormal device characteristics was detected while measurements were taken of six transistors located in the memory cell of the SRAM. In comparison with normal transistors adjacently located, this

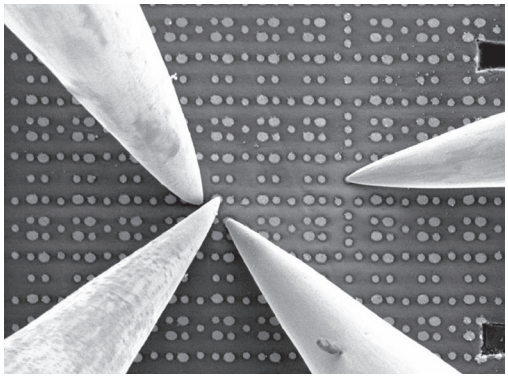

Photo 3 Taking measurement using a nanoprobe.

transistor shows an abnormality with a significantly low current when turned on.

When the cross section of the defective transistor was analyzed by viewing it through a transmission electron microscope (TEM) device for the distribution of dopant, using high sensitivity TEM-EDS analysis method, an abnormality with a distribution of dopant was determined (**Photo 4**).

With the progress in physical analysis technology, abnormalities with transistors in LSIs, which were difficult to analyze with conventional failure analysis, can now be clarified. The technology has recently become an essential technology for ensuring the quality of LSIs.

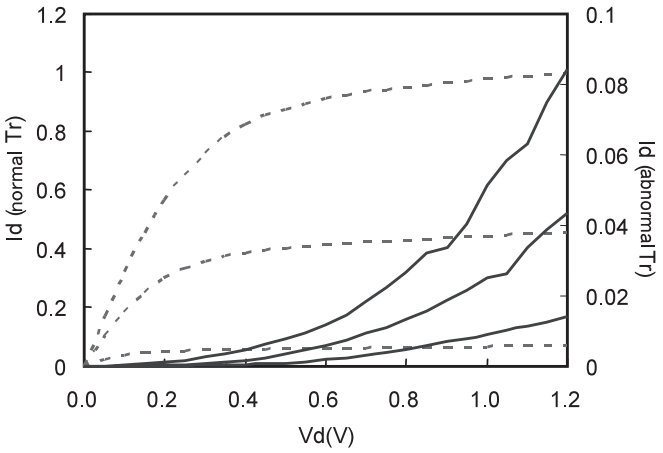

Fig. 8 Result of measurement for characteristics of transistors inside defective memory cell of an SRAM. Black lines represent normal and blue lines represent abnormal transistor characteristics.

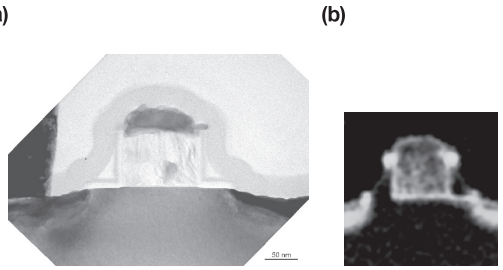

Photo 4 Result of cross sectional observation using TEM device of transistor with abnormal characteristics and result of TEM-EDS mapping analysis for dopant distribution.

5. Conclusion

In order to analyze the failure of advanced devices in short periods of time, it is necessary to seamlessly and efficiently connect failure diagnosis to physical failure analysis using design data, as described above. Since further acceleration in the rate of miniaturization to microscopic sizes and further expansion on a large scale are expected to continue for devices in the future, it is necessary to further develop failure analysis technologies for which comprehensive technical capabilities are assessed. It is for this reason that we intend to (1) develop diagnostic technologies for various faulty cases in practice with high precision and high speeds, (2) implement devices for high precision analysis and develop measuring technologies, as well as (3) firmly promote the development of analysis devices.

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