A Fast Board-Power-Voltage Fluctuation Analysis System for Chip-Package-Board Co-Design

By Takashi HARADA,* Hiroshi WABUKA,* Manabu KUSUMOTO,* Masatoshi OGAWA,* Shunji SATOH† and Junji KOSUGE†

ABSTRACT Recent progress trend in electronics supported by high-speed signal processing of semiconductor chips and high-density packaging technologies reduce layout margins and bring packaging design difficulties. To reduce the time loss by the rework and increase packaging design efficiency in the early stage of product development, short turnaround-time estimation techniques for analyzing the electrical performance integrating chip-package-board characteristics have been required. This paper describes a fast board-power-voltage fluctuation analysis system to realize the chip-package-board co-design.

KEYWORDS **LSI chip, LSI package, Printed circuit board, Co-design, Power integrity**

1. INTRODUCTION

Recent progress in electronics is supported by high-speed signal processing of semiconductor chips and high-density packaging technologies[1]. However these trends reduce layout margins and bring packaging design difficulties. For example, the transmission speed between a CPU and memories has become almost 100 times faster in this decade. The switching speed has been progressed from nano seconds to several tenths of pico second. The propagation distance of electric signal is 1.5 - 1.8mm per 10ps, so the board and LSI package layout should be adjusted in the mm range to secure normal circuit operation. Since the size of an LSI is generally several tenths of mm square, not only board but also LSI package design including trace layout and pin assignment should be considered.

Charge supply to the LSI chip is another problem. Switching of the LSI chip is achieved by charge to and discharge from LSI loads. These charges are mainly supplied by SMT capacitors and power voltage regulators on the board. Appropriate power distribution (charge supplying) system has to be achieved to prevent circuit troubles, such as circuit malfunctions and speed drops. In the low speed switching age, these charges could be supplied from capacitors or voltage regulator modules on the entire board. In the high speed switching, however, the charges can only be supplied by capacitors mounted very close to the LSI. Appropriate capacitor allocation near the LSI is very difficult due to high density trace layout.

On the other hand, **Fig. 1** shows a flowchart of electronic product development. An LSI design and a board design are processed separately. Moreover, the chip and the package in the LSI designs are separated, considering the chip and the product specification. After combining the chip and package design

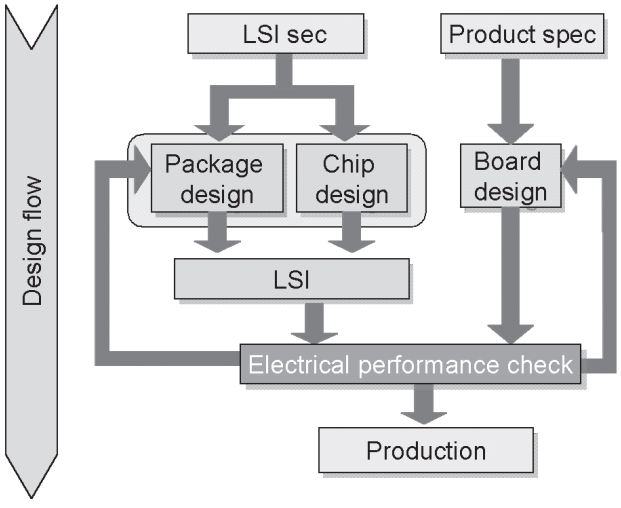

Fig. 1 A flowchart of electronic product design and development.

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outputs, electric characteristics of the LSI can be decided, and the board layout is designed by using the information on LSI characteristics. In this process, the final performance can be confirmed after whole designs have been finished. Finding out any troubles at this stage, however, requests the board layout re-design and the package layout re-design. It sometimes requires going back to reconsiderations of the LSI specification. This rework is one of the main reasons for development delays. To give full performance of chips which are advanced year by year, and provide new products to market without any delays by reducing development period, the package and the board layout design considering a chip-package-board co-design concept should be applied in the early development stage.

Since the detail layout of the LSI packages and the boards have not been decided yet at the beginning of development, the restrictions from practical layout conditions are small. On the other hand, the arranging components and trace wiring by grasping the electrical characteristics are necessary. Circuit simulators or full-wave simulators are principal methods to evaluate the electrical performance. Analysis using these simulators, however, takes several hours or several days, therefore they are not suitable for analysis in early design stage, for which real-time responses are required.

Consequently, to reduce the time loss by the rework and increase design efficiency in the early stage of product development, short turnaround-time estimation techniques for analyzing the electrical performance integrating chip-package-board characteristics have been required. This paper describes a fast board-power-voltage fluctuation analysis system to realize the chip-package-board co-design.

2. FRAMEWORK

The framework of this system is shown in **Fig. 2**. For the board estimation purpose, the system is composed of two modules, LSI modeling module, and board modeling and analysis module. The LSI modeling module extracts equivalent circuit models of a chip and a package from chip operation information and package layout data. The module treating a board extracts the equivalent circuit model from board layout and then analyzes board characteristics quantitatively by using the LSI equivalent circuit. The behaviors of the LSI and board are expressed as equivalent circuits, because widespread circuit simulator SPICE (Simulation Program with Integrated Circuit Emphasis) is used as an analysis engine.

At the beginning of new product development, LSI specifications are almost fixed, so this system configuration is effective for estimating the dependence of the board layout on total chip-package-board system characteristics. This paper mainly introduces the power distribution characteristics analyzing method to design the power-plane layout of the board and decoupling capacitor allocation. The characteristics are evaluated by power-voltage fluctuations.

3. EXTRACTING EQUIVALENT CIRCUIT MODELS

3.1 LSI Modeling

Figure 3 shows the equivalent circuit model of an LSI (a chip and a package) for analyzing the power-voltage fluctuations by arranging board layout. This model is composed of a current source and lumped circuit elements. The current source describes the

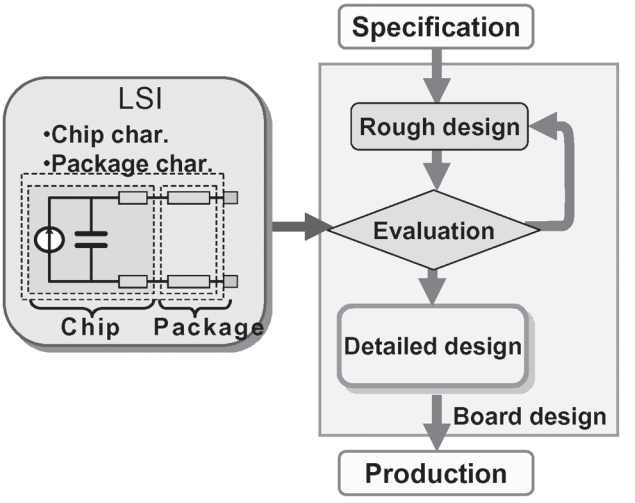

Fig. 2 Framework of analysis system integrating chip, package, and board characteristics.

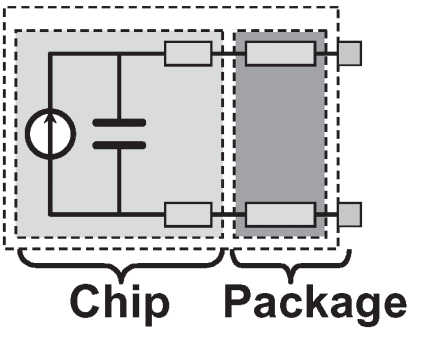

Fig. 3 Equivalent circuit model of an LSI.

time transition of charge demands by the chip switching operation, and the lumped circuit elements are extracted from traces in the chip layout and the package layout[2].

The current-source model is extracted as follows. At first, the SPICE based time-domain transistor net list is constructed from the whole chip circuit information. Then, time-domain wave form of the current is calculated by SPICE transient analysis as shown in **Fig. 4**. The trace models of the chip and the package are expressed as lumped circuit elements, L, R, and C which are calculated by a two-dimensional field solver.

3.2 Board Modeling

Since the board is extended in two dimensions, the board model can be expressed as the tow-dimensional equivalent circuit network as shown in **Fig. 5**. The model consists of the two-dimensional array of impedance Z, and admittance Y. These parameters are extracted by dividing a power and ground plane pair into square capacitive/conductive cells and square inductive/resistive cells[3,4].

$$Z = R + j\omega L \quad (1)$$

$$Y = \omega C \tan\delta + j\omega C \quad (2)$$

C, L, and R are;

$$C = \varepsilon_r\varepsilon_0 + \frac{l^2}{d}, \quad (3)$$

$$L = \mu_0 d, \quad (4)$$

$$R = 2\frac{\rho}{t}, \quad (5)$$

where ε_r, ε_0, μ_0, ρ, d and l are the relative permittivity of the dielectric, the permittivity in free space, the permeability in free space the conductivity of plane conductor, the space between power and ground planes, and the side length of the cell. This extraction can be effective when the board thickness is sufficiently smaller than the wave length of consideration[5]. In this case, the electromagnetic wave propagates only in the plane direction.

3.3 Frequency Domain Analysis

To achieve short turnaround analysis, proposed system adopts frequency-domain analysis method, as shown in **Fig. 6**, instead of conventional transient analysis. Normally, power-voltage fluctuations in the

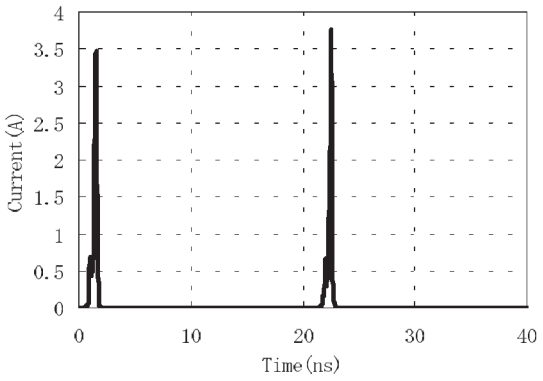

Fig. 4 LSI power pin current wave form (time domain).

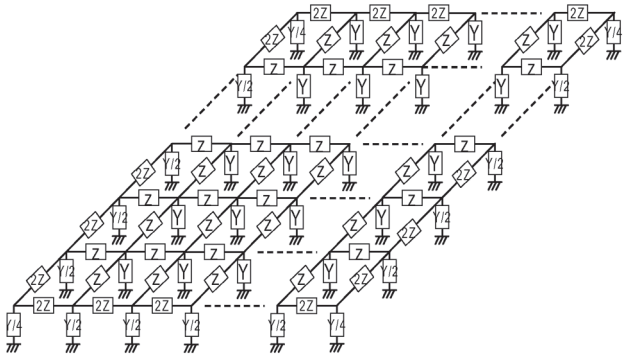

Fig. 5 Two-dimensional equivalent circuit network of power-distribution planes.

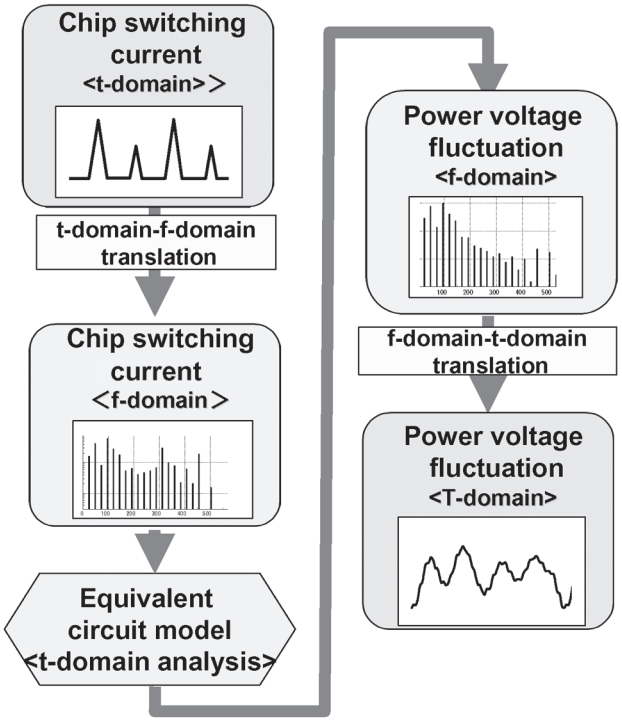

Fig. 6 Flowchart of fast power-voltage fluctuation analysis.

chip-package-board system are calculated by transient analysis which calculates time sequential phenomenon step by step. Since this method repeats calculation until the system becomes stabilized (more than 1 million times), it takes several hours.

The frequency analysis, however, needs calculation of some specific frequency points: basic clock frequency and several harmonic frequencies. This approach is based on the feature that the power-voltage wave form is repeated by a cycle coinciding with the clock frequency. Generally, the calculation points should be the fundamental clock frequency and harmonic frequencies up to 30 harmonics. This idea can drastically reduce analyzing time.

4. POWER-VOLTAGE FLUCTUATION ANALYSIS

The four-layer printed circuit board fabricated for this analysis was 300 × 200mm in size and 1.6mm thick (see **Fig. 7**). The board was composed of four layers. The second and third layers were assigned for a ground plane and a power plane, respectively. The space between the two internal planes was about 1mm. The planes were made by 30μm copper sheet. This board contained pairs of pads that mounted capacitors used to interconnect these two planes with via holes. An LSI having a typical switching function was mounted on the board. The clock frequency of operation was 24MHz.

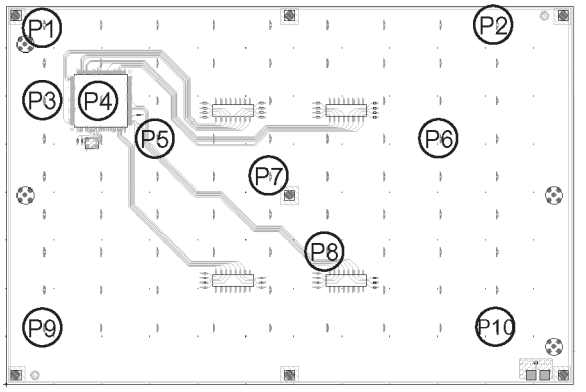

Fig. 7 Board under test.

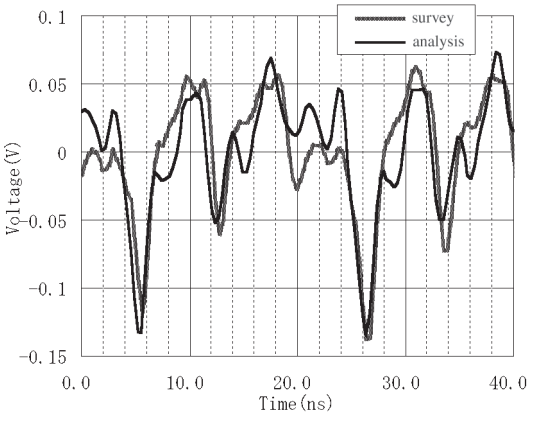

Fig. 8 Power-voltage fluctuation.

Nine decoupling capacitors were mounted on the opposite surface of the LSI. One capacitor was directly under the LSI and other eight capacitors were mounted to surround the LSI. The capacities of all capacitors were 0.1μF. The effect of the decoupling capacitor was expressed as an equivalent circuit model consisting of capacitance, resistance and inductance; the capacitance of the capacitor, equivalent series resistance of the capacitor, and interconnect inductance associated with an equivalent series inductance of the capacitor and inductance of pads and via holes[6].

Figure 8 is the power-voltage wave form at the point of the LSI center (P4). The thin line shows calculation result achieved from this system. Repetition time is about 42ns which is a reciprocal of clock frequency. The thick line shows the experimental result. These lines relatively agree. The peak-to-peak voltage fluctuation which is especially important factor for circuit operation can be expressed well. The analysis time was several tenths of second. This turnaround time is about 100 times faster than conventional transient analysis method, in spite of including time-domain to frequency-domain translation and frequency-domain to time-domain translation process.

Comparison of the analysis results of the peak-to-peak voltage with the experimental ones at several positions throughout the board (from P1 to P10) shows the deviations less than 20%. The maximum error was 20mV, which is accurate enough for application in early design stage.

5. CONCLUSION

A fast board-power-voltage fluctuation analysis system to realize the chip-package-board co-design has been introduced. This system contributes to the increase of design efficiency in the early product development stage followed by reducing the time loss due to the rework in the development process. At the present time, the role of electronic product development is parted by LSI vendors and product manufactures; the chip and the package design is

performed by LSI vendors, and the board design is done by product manufactures. In future, however, the collaboration in the early development stage will become a matter of great demands to increase design efficiency and reduce the development period. The system described here will play an important role in this scene.

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