High-Performance FCBGA Based on Ultra-Thin Packaging Substrate

By Katsumi KIKUCHI,* Jun SAKAI,* Koichiro NAKASE,* Hideya MURAI,* Hirobumi INOUE,* Hirokazu HONDA,† Keiichiro KATA† and Kazuhiro BABA*

ABSTRACT We developed a high-performance Flip-Chip Ball Grid Array (FCBGA) based on an ultra-thin, high-density packaging substrate called a Multi-Layer Thin Substrate (MLTS) in order to meet the high demand for high-density, high-performance, and low-cost LSI packages. The most important feature of the package is that it has a high-density, high-performance MLTS formed by removing a metal plate after mounting an LSI chip on it. A prototype high-density FCBGA exhibited excellent long-term reliability. The electrical simulation results indicate that the MLTS packaging technology has the advantage of excellent high-frequency properties compared with a FCBGA using a conventional build-up PWB substrate.

KEYWORDS **Flip-chip, BGA, High-density, Ultra-thin, Packaging substrate**

1. INTRODUCTION

The greater numbers of I/O pads, increasing I/O pad-density, and higher operation frequencies of recently developed high-performance ASIC chips have created a strong demand for high-density and high-performance FCBGA packages. **Table I** shows technology requirements for high-performance and higher-pin-count area array FCBGA packages[1]. The table tells us that in the near future, FCBGA packages will require packaging substrates having fine-pitch lines smaller than 30μm, and 30μm via-hole diameters. The packaging will also have to support an operation frequency of at least 1GHz, and a reasonable production cost. In addition, packaging substrates have to feature excellent flip-chip mounting reliability, which makes high-pin-count and 120μm-pitch area array flip-chip interconnection possible.

Conventional FCBGA packages are made of build-up printed wiring boards (PWBs)[2]. However, conventional build-up PWBs have the following problems: 1) the existence of through-holes in the core laminate has been an obstacle to higher-speed and higher-frequency applications, because through-holes prevent impedance matching; 2) the curvature and unevenness of the core laminate have become the limiting factor in achieving the fabrication of high-density substrates; and 3) the deficiency of core laminate stiffness has required building up layers on both sides, which increases the production costs. To meet the future technology requirements, we developed a new multi-layer thin-substrate (MLTS) packaging technology[3-4].

This paper describes the concept of MLTS packaging, the process technology, the production of a prototype device, the evaluations of its long-term reliability, and the high-frequency properties.

2. MLTS PACKAGING CONCEPT AND ADVANTAGES

Figure 1 shows the concept of the MLTS packaging technology. The important point is to apply a high-density, high-performance MLTS without

Table I Technology roadmap for LSIs and FCBGA packaging substrates.

Year of Production	2003	2004	2005	2006	2007
LSI					
Design Rule (μm)	0.11	0.09	0.08	0.07	0.065
Pad Pitch - Area Array (μm)	150	←	130	←	120
Number of Pads	3400	3600	4000	4200	4400
Clock Frequency (GHz)	3.1	4.0	5.2	5.6	6.7
Package					
Number of Pins	2,060	2,260	2,490	2,740	2,740
Substrate Wiring Pitch (μm)	36	←	30	←	28
Substrate Via Diameter (μm)	40	←	30	←	25
Cost (cents/pin)	2.0	1.9	1.8	1.7	1.6

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through-holes for the packaging substrate, in place of a conventional build-up PWB. **Figure 2** shows the conceptual fabrication process flowchart that we developed. The process consists of MLTS fabrication on a metal plate, an LSI chip mounting on the metal-base MLTS, and the metal plate removal in order to leave only a high-density MLTS, and finally the attachment of a heat spreader and solder balls.

Figure 3 summarizes the advantages of the MLTS packaging. The MLTS packaging has interesting characteristics such as the use of a rigid, very flat, metal-base substrate as a support plate up until the LSI chip mounting is executed, a through-hole-less multi-layer structure, and a structure with fewer layers fabricated with fine-pitch patterning. Such interesting characteristics will produce the following advantages: (1) good registration accuracy, which makes higher-density and finer-pitch patterning possible; (2) excellent flip-chip mounting reliability, which makes higher-pin-count and finer-pitch area array flip-chip interconnection possible; (3) excellent reliability, supported by the use of high glass transition temperature (Tg) resin such as polyimides; (4) an ideal multi-layer structure that is highly suitable for high-speed and high-frequency applications; and (5) a cost-effective design achieved as a result of fewer layers fabricated with fine-pitch patterning.

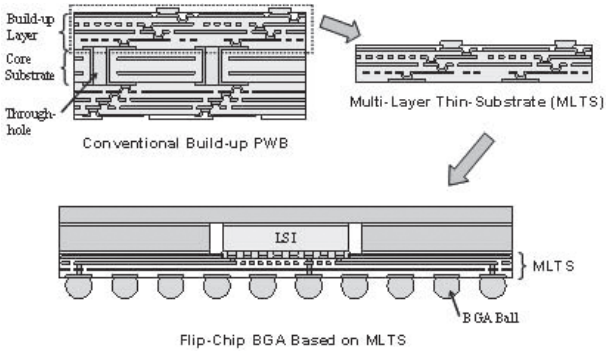


Fig. 1 Concept of MLTS packaging technology.

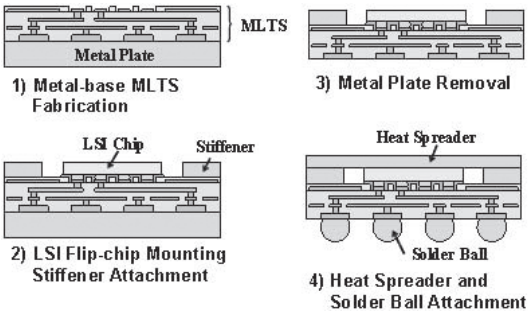


Fig. 2 Conceptual fabrication process flowchart for MLTS package.

3. FCBGA PACKAGING TECHNOLOGY

3.1 Packaging Substrate Fabrication Process

Figure 4 shows the fabrication process flowchart for the MLTS. In this examination, we used a 0.5mm-thick Cu plate for lead frame materials. After first

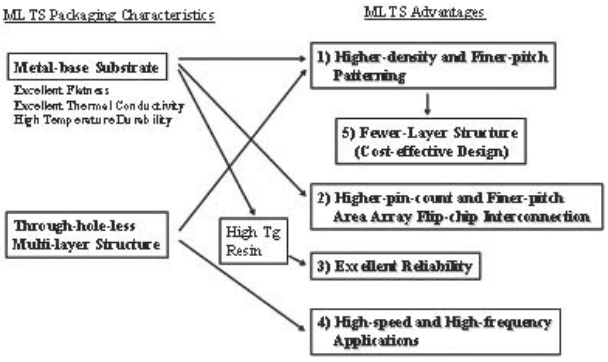


Fig. 3 Advantages of MLTS packaging technology.

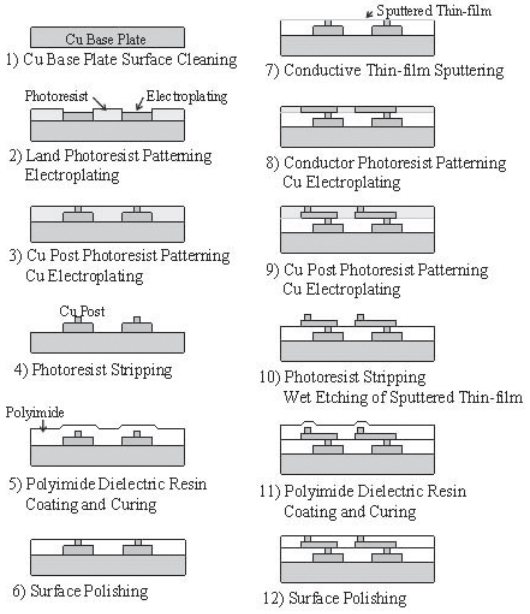


Fig. 4 Fabrication process flowchart for MLTS.

cleaning a Cu plate surface, we applied photoresist patterning and electroplating to fabricate BGA lands. To fabricate the BGA lands, we piled up Ni, Au, Ni, and Cu electroplating layers on a Cu plate. The Au layer functioned as barriers during the Cu plate etching. The Ni layers were also effective in preventing Au-Cu diffusion. Then, we used photoresist patterning and Cu electroplating to create a Cu plating post that will correspond to via-hole positions. Next, the dielectric resin was deposited, cured, and polished down to the tops of the Cu plating posts.

Fine-pitch Cu conductor layers were fabricated through a semi-additive process with a sputtering method[4,5]. This process combines the deposition of a conductive sputtered thin-film, a high-resolution photoresist patterning, Cu electroplating, photoresist patterning for posts, Cu electroplating, photoresist stripping, and wet etching of the sputtered thin-film.

The dielectric fabrication was a very simple process involving coating, curing, and surface polishing. In this study, we examined polyimides because they have excellent mechanical properties, good electrical performance, and high Tg. **Table II** shows typical properties of the polyimide used for the MLTS fabrication.

Table III summarizes the specifications for the MLTS. Good registration accuracy, supported by the use of a metal-base substrate, made higher density fabrication easier. The MLTS made it possible to produce 20μm pitch lines with 30μm diameter via-holes and 50μm diameter lands at a practical level, as shown in **Fig. 5**. Such high-density design rules will be applied even to future fine-pitch area array LSI chips.

Table II Typical properties of polyimide used for MLTS fabrication.

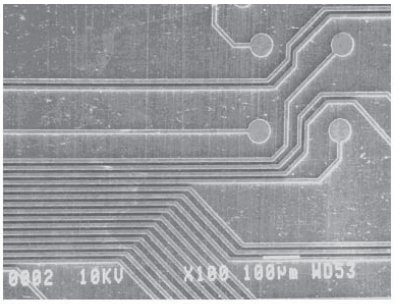
Tensile Strength	400 Mpa
Elastic Modulus	4.7 GPa
Elongation	50%
Dielectric Constant (1 MHz)	3.1
Dissipation Factor (1 MHz)	0.002
Thermal Coefficient of Expansion	21 ppm / ℃
Glass Transition Temperature	> 300 ℃
Curing Temperature	350 ℃
Water Absorption	1.0 wt%

Table III Specifications of MLTS.

Multi-Layer Design Rule	
Line Width / Space	10 µm / 10 µm
Via-hole (metal-filled) / Land Diameter	30 µm / 50 µm
Via-hole Pitch	60 µm
Metal Plate	Cu
Dielectric Resin	Polyimide
Adhesive Strength of Metallization	0.7 kN / m (Peel Strength)
Characteristic Impedance	50 - 52 Ω
Propagation Delay Time	62 ps / cm

3.2 Prototype

We successfully developed a high-density flip-chip BGA prototype based on our MLTS packaging technology. **Figure 6** shows cross-sectional photographs of the prototype. The prototype is composed of an LSI chip connected to approximately 2,500 bonding pads arranged in a 240μm-pitch area array, and 1,296 I/O pads for BGA. **Table IV** compares its specifications with those of an identically functioning build-up PWB. It should be noted that the MTLS prototype consists of only four conductor layers due to its high-density design rules (40μm line pitch, 40μm via-hole



Line Width / Space = 10 µm / 10 µm
Land Diameter = 50µm

Fig. 5 SEM photograph of Cu wiring lines in MLTS.

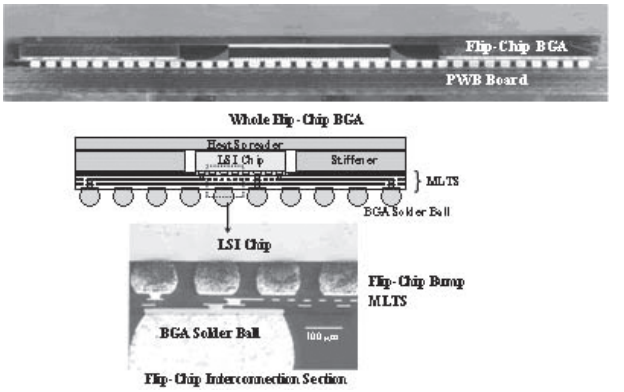


Fig. 6 Cross section of FCBGA prototype.

diameter), while a build-up PWB needs 12 conductor layers. The prototype's MLTS has an eighth part time as thin as a build-up PWB, and a hardly seen MLTS with a whole package size view, as shown in Fig. 6.

Since our prototype has fewer conductor layers than a build-up PWB, the MLTS packaging is considered to be the best solution for enabling high-speed and high-frequency signal transmission, all using a cost-effective design.

3.3 Reliability

We evaluated the reliability of the flip-chip BGA based on our MLTS packaging through a series of long-term reliability tests. Test results obtained are shown in **Table V**. The prototype's excellent long-term reliability was demonstrated through a series of tests conducted on it: reflow resistance test (30°C, 70%RH, 192h/240°C reflow three times), package level thermal cycle test (–40°C, 30min/+125°C, 30min, 1,000 cycles), package on board (1.6mm thick, four conductor layers, 150mm by 120mm in size) thermal cycle test (–40°C, 30min/+125°C, 30min, 1,000 cycles), and highly humidity bias test (85°C, 85%RH, 10V, 2,000h).

Table IV Specifications for FCBGA prototype.

	MLTS	Build-up PWB
Substrate Design		
Line Width / Space	20 µm / 20 µm	40 µm / 40 µm
Via-hole / Land Diameter	40 µm / 80 µm	60 µm / 100 µm
Dielectric Layer Thickness	25 µm	60 µm
Conductor Layer Thickness	10 µm	15 µm
Number of Conductor Layers		
Total (Top / Core / Bottom)	4 (3/1/0)	12 (4/4/4)
Signal Layer	1	2
Substrate Total Thickness	0.11 mm	0.80 mm
FCBGA Package Design		
Number of Flip-chip Pads	2500	
Flip-chip Pad Pitch	240 µm	
LSI Die Size	11 mm □	
Number of I/O Pads for BGA	1296	
I/O Pad Pitch	1.0 mm	
Package Size	37.5 mm □	

Table V Results of long-term reliability tests.

Test Item	Test Condition	Result
Package Level		
Reflow Resistance	30 °C / 70%RH, 192 hr, Max. 240 °C reflow 3 times	**Pass (n=22)** (No Crack, No Blister)
High Temperature & Humidity Bias Test	85 °C, 85%, 10V	**2000 hr Pass (n=12)** (Insulation Resistance > 10^9 Ω)
Thermal Cycle Test	-40 °C, 30 min / +125 °C, 30 min	**1000 cyc. Pass (n=12)** (No Crack, Resistance Variations < 10%)
Package on Board Thermal Cycle Test	-40 °C, 30 min / +125 °C, 30 min	**1000 cyc. Pass (n=16)** (No Crack, Resistance Variations < 10%)

In future work, we intend to verify the reliability of a prototype fabricated with Pb-free solder bumps and balls in the same manner.

4. HIGH-FREQUENCY PROPERTIES SIMULATION

The MLTS structure without through-holes will be suitable for higher data transmission. We evaluated the high-frequency properties of the MLTS and the conventional build-up PWB by using a simulation carried out on a 3D-electo-magnetic simulator with the FITD algorithm (Microwave Studio).

The package size was set at 50×50mm, and the S-parameters of the transmission line between the FC pad and BGA land were calculated by the simulator. The length of the transmission line (strip line) was 35mm (= 50mm/2×$\sqrt{2}$), which was the distance from the center to a corner of the package. The signal was fed by power ports; port1 was attached to an FC pad and port2 was attached to a BGA land. **Figure 7** and **Table VI** show the simulation models and design parameters.

The return loss (S11) and insertion loss (S21) calculated by the simulator are shown in **Fig. 8**. The resonance appeared to correspond to the 35mm transmission line because reflection occurred at the connection part of transmission line and via-hole structure. The insertion loss resonance occurred in

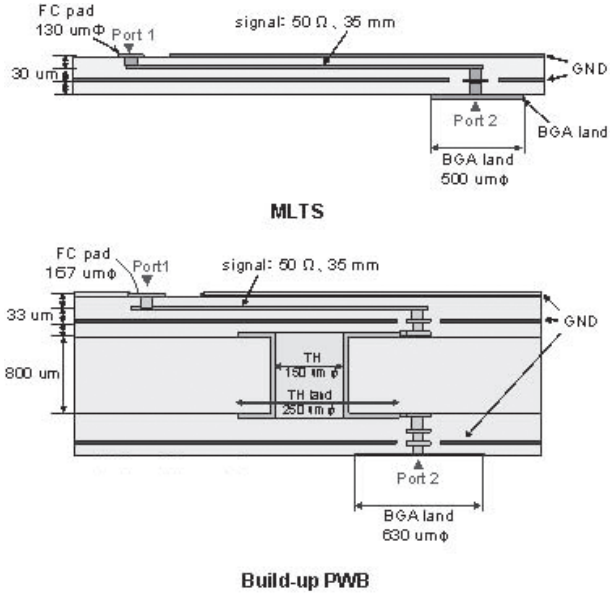


Fig. 7 Simulation models for MLTS and build-up PWB.

the via-holes structure. To ignore this resonance in quantitative comparison, approximated curves of the least square method were inserted in the figures. The losses for the MLTS were smaller than those for the build-up PWB.

We then conducted an in-depth analysis of the MLTS high-frequency properties.

The electric-field distributions around the BGA land in both devices are shown in **Fig. 9**. While the field in the MLTS is uniform, that in the build-up PWB is not uniform at the interconnection of the via-holes and through-holes. The through-holes in the build-up PWB are much larger than the via-holes, resulting in electrical discontinuity at the interconnection. This discontinuity is thought to generate unnecessary losses and to degrade the transmission characteristics. Therefore, the existence or nonexistence of through-holes is considered to be the factor in the difference.

Figure 10 shows dividing models and simulation results. To verify the degree of the influence of through-hole to the characteristics of the whole package, the simulation models shown in Fig. 7 were divided into two parts. Part (a) included an FC pad and a 31mm long transmission line, and part (b) included a 4mm long transmission line and a BGA land. For part (a), with no through-hole, no differences were evident between the properties of the two packaging substrates. For part (b), which included a through-hole, the insertion loss of the build-up PWB was larger than that of the MLTS. Therefore, these simulation results clearly show that the most dominant reason of the difference in signal integrity is the absence of through-holes in the MLTS.

Table VI Design parameter for simulation models.

	MLTS	Build-up PWB
Substrate Design		
Line Width / Space	20 µm / 20 µm	40 µm / 40 µm
Via-hole / Land Diameter	40 µm / 60 µm	60 µm / 100 µm
Dielectric Layer Thickness	25 µm	60 µm
Conductor Layer Thickness	10 µm	15 µm
Number of Conductor Layers		
Total (Top / Core / Bottom)	4 (3/1/0)	12 (4/4/4)
Signal Layer	1	2
Substrate Total Thickness	0.11 mm	0.80 mm
FCBGA Package Design		
Number of Flip-chip Pads	2500	
Flip-chip Pad Pitch	240 µm	
LSI Die Size	11 mm □	
Number of I/O Pads for BGA	1296	
I/O Pad Pitch	1.0 mm	
Package Size	37.5 mm □	

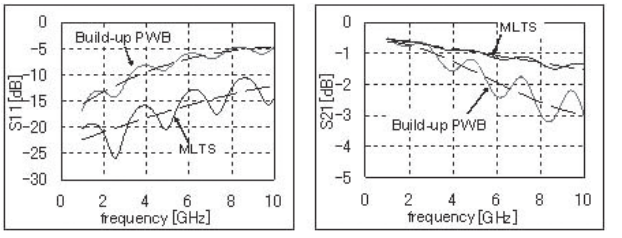
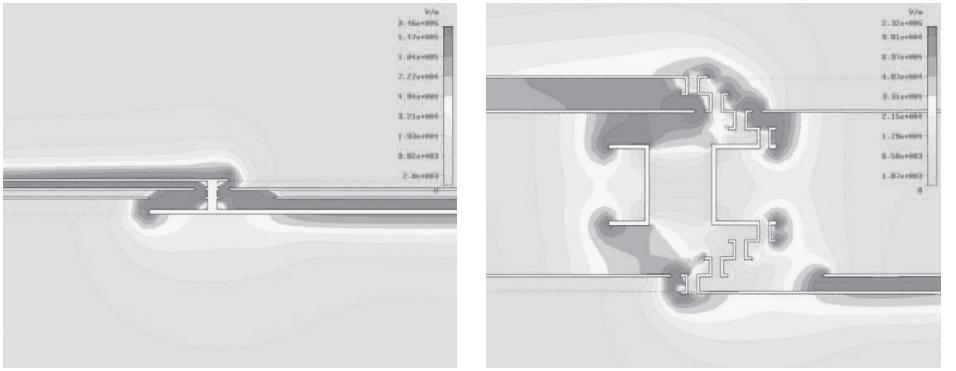


Fig. 8 Simulation results.



(a) **(b)**

Fig. 9 Electric-field distribution in (a) MLTS, and (b) build-up PWB.

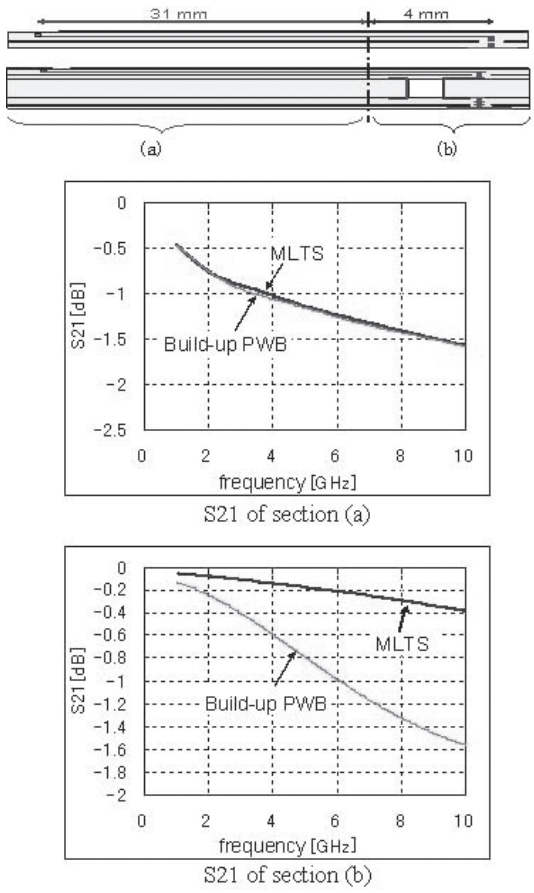


Fig. 10 Divided models and the S21 of each section.

5. CONCLUSION

We developed a FCBGA based on MLTS packaging technology in order to meet the strong demand for high-density and high-performance flip-chip BGAs. The MLTS packaging has the following advantages: (1) good registration accuracy, which makes higher-density and finer-pitch patterning possible; (2) a structure without through-holes that is highly suitable for high-speed and high-frequency applications; (3) excellent flip-chip mounting reliability, which makes higher-pin-count and finer-pitch area array flip-chip interconnection possible; (4) excellent reliability, supported by use of a high Tg resin such as polyimides; and (5) a cost-effective design achieved as a result of fewer layers fabricated with fine-pitch patterning. We successfully developed a high-density flip-chip BGA prototype based on our MLTS packaging technology. The prototype's excellent long-term reliability was also demonstrated through a series of tests conducted on it. We observed that our MLTS has excellent high-speed signal transmission properties by using a 3D-electo-magnetic simulator with the FITD algorithm.

Our next goal will be the production release of MLTS packages, which will meet a high operating speed (> 10GHz) application requirement.

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