C-based High Level Synthesis and Verification Tool Set for ASIC / FPGA
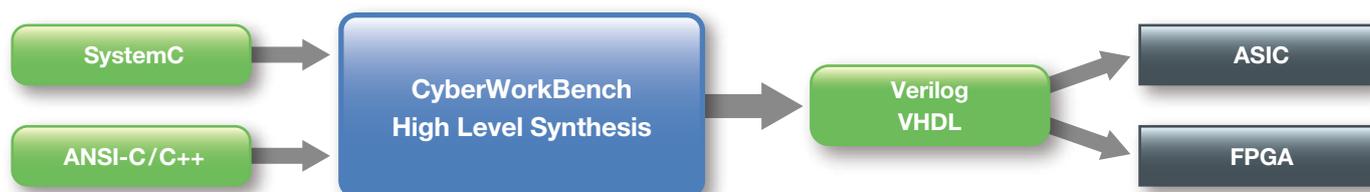
CyberWorkBench®

Pioneering C-based LSI Design

C-based Design Enables Higher Design Efficiency, Lower Area and Higher Performance of Your Chip

(compared to RTL-based design)

Best-in-class High Level Synthesis and Verification used over 20 years for real chip design

SystemC → CyberWorkBench High Level Synthesis

ANSI-C/C++ → CyberWorkBench High Level Synthesis

CyberWorkBench High Level Synthesis → Verilog VHDL
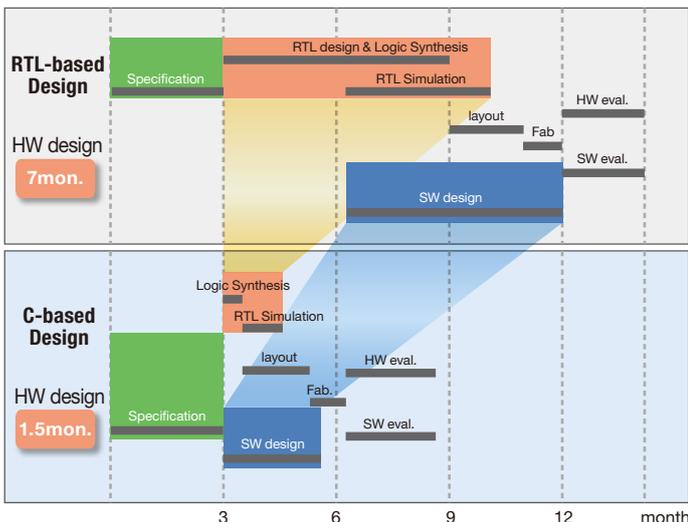
Verilog VHDL → ASIC

Verilog VHDL → FPGA

CyberWorkBench provides "All-in-C" synthesis and verification:
Any type of module (controller or datapath) can be synthesized and verified at the original C-level.

Adavantages

Design Cost Reduction:

- Description reduction:5-30%, simulation speed 100X
- Design man-month reduction(e.g.80MM –> 10MM)
- Design period for HW (blue)and SW(red) are both reduced
- Higher reliability: fast HW-SW co-verification(cycle accurate)

RTL-based Design
HW design
7mon.
Specification
RTL design & Logic Synthesis
RTL Simulation
layout
Fab
HW eval.
SW design
SW eval.

C-based Design
HW design
1.5mon.
Specification
Logic Synthesis
RTL Simulation
layout
Fab.
HW eval.
SW design
SW eval.

3   6   9   12   month

Chip Cost Reduction: Smaller Area/Power

- HLS can generate smaller and lower power designs compared to manual RTL designs through maximum resource sharing
- Area and performance optimization for Altera, Xilinx FPGA

Chip — Area Reduction → Chip
RTL-based   C-based
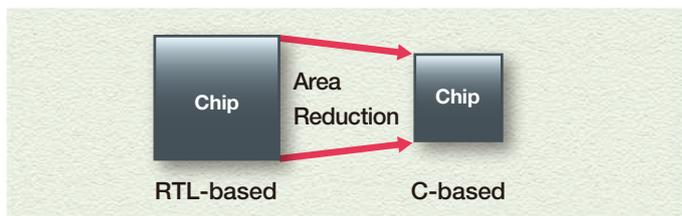
Application

- Digital Circuits: mobile phone, base station, computer, transmission equipment, STB, digital camera, printer, controllers
- Acceleration of server: Big data (e.g. High Frequency Trading)
- Replacement of real time processing MPU: sensor monitoring and motor control
- Controller: Factory Automation, Medical, Automobile

CyberWorkBench Editions

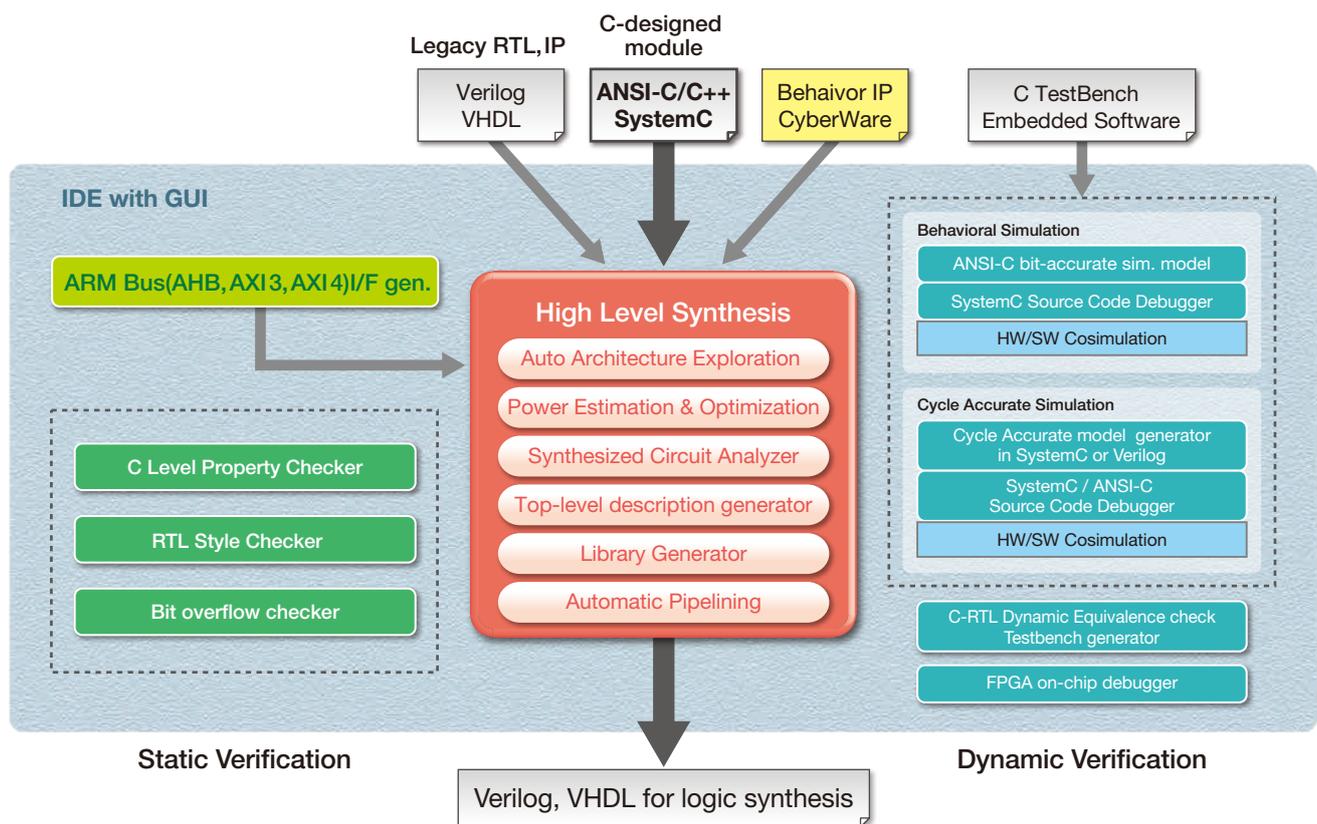| Edition	Enterprise	Professional	Standard	Basic
Target	ASIC / FPGA	FPGA	FPGA	FPGA
Limitations	none	none	input size/device	input size/device

Tools in CyberWorkBench

"All-in-C" Synthesis

- Any types of modules including control dominated circuits and datapath
- Best-in-class High Level Synthesizer (automatic pipelining, power optimization, powerful parallelism extraction, multiple clock domains, various types of circuits and memories, fixed point, sync/asyc, etc.)
- Automatic micro-architectural exploration
- Powerful graphical analysis capabilities for synthesized circuits
- Automatic top level structural description generator which connects C-designed modules and RTL legacy modules.
- Supports any ASIC technology and Altera/Xilinx FPGAs
- Includes numerous behavioral IPs (CyberWare) easily retargetable for area or performance

"All-in-C" Verification

- Assertions described in the C source code are automatically translated into RTL assertions for formal verification and RTL simulation
- SystemC source code debugger makes SystemC debug much easier than g++ debugger (e.g. gdb)
- C source code debugger for timing verification directly at the ANSI-C/SystemC sorce code
- Legacy/RTL, IP conversion into SystemC for integration with newly developed C/SystemC modules
- Testbench generator allows re-usage of untimed C stimuli in cycle-accurate and RTL simulation
- Test pattern can be described directly at the C level. HW-SW co-simulation with CPU vendor's ISS

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