

Logic LSI Yield Improvement Analysis By Means of Fault Diagnosis

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Abstract

Advancements consequent on the increase in functions and the decrease in the size and weight of home electrical appliances and various related devices have been promoting improvements to the micro-fabrication technologies. This trend is tending to bring about increases in the scale of the LSIs that are used in them. In the case of the LSIs, it is extremely important to ramp up and maintain a high yield from the start of production and to supply high-quality products stably both from the viewpoints of acquiring customer confidence and of securing profits.

This paper is intended to introduce a fault identification technology, which is an innovation that features a pinpoint identification capability. This solution is important in quickly clarifying the causes affecting the yield. Some aspects of actual cases are also examined.

Keywords

LSI, logic circuit, yield, fault, analysis, diagnosis

1. Introduction

Activities for improving yield and quality by applying various analyses are conducted routinely at the LSI production lines. In order to manufacture products at high yields the production line workforce accumulates the results of in-line monitoring and testing as continuous statistical data. By analyzing these data with a data mining technology and identifying the common factors of periodic variations and yield degradation from correlations of manufacturing equipment and recipes, etc. they can then apply the requisite countermeasures. In the case of a sudden drop in yield, the wafer in question is analyzed to identify the cause of failures in the defective LSIs.

Factors that affect the process and reduce the yield are thus identified and the necessary countermeasures are applied in order to prevent their recurrence (Fig. 1).

In the case of the memory circuit, identification of the cause of a fault is relatively easy because the address of the faulty cell can be found from the test results. Therefore, the improvement of the overall yield of LSIs has previously been attempted by analyzing the memory circuit. However, as the increases in scale and integration have tended to increase the weight of the logic circuit, the yield of the logic circuit has tended to have a greater effect on the overall LSI yield than previously. Thus, the importance of performing logic circuit analyses is increased.

On the other hand, recent LSIs have been designed using the

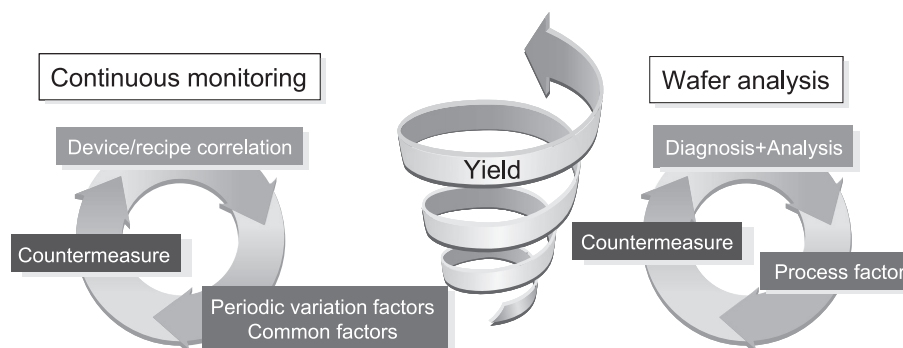


Fig. 1 Yield analysis.

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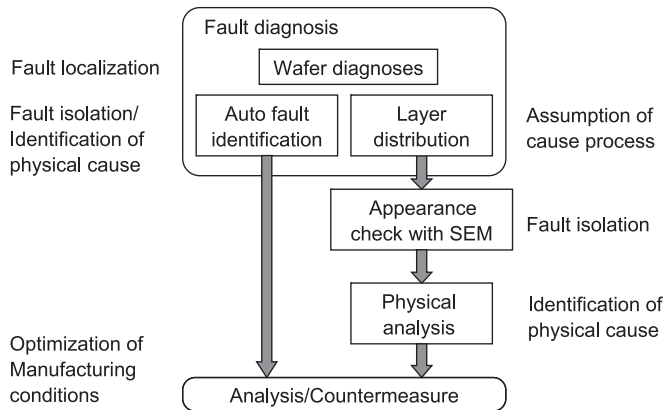


Fig. 2 Flow of failure analysis for yield improvement.

high-level language such as behavioral description. As the circuit and manufacturing mask data are generated automatically as well as the test data for shipment inspections, even the designers tend to have difficulty in understanding the relationship between the circuit configurations and the functions of the actual devices. In addition, failure analysis (FA) for identifying cause of failures is also becoming more demanding because of the advances in the micro-fabrication methods. This has caused the sizes of the fault to approach the resolution limits of FA equipments.

To deal with these circumstances, FA engineers in NEC Electronics effectively utilize fault diagnosis technology that can localize the faulty block with high accuracy, which enables them to identify the causes of yield degradations over short periods¹⁾. In the following sections, we will introduce two fault diagnosis techniques; 1) A technique for identifying the fault sites without physical failure analysis and 2) A technique for identifying the fault sites efficiently by assessing the cause from the diagnosis results and selecting samples to be subjected to failure analysis (Fig. 2).

2. Auto-Identification of Fault Sites

In the manufacturing process, the manufacturing conditions are confirmed in every main process by inspecting shape anomalies in wafers by using defect inspection systems and recording the inspection results. The shape anomalies detected in the inspections do not always affect the quality of product but some of them may lead to logic errors and thus cause faults. Yield improvement necessitates clarification of the causal relationship between shape anomalies and product yield and the

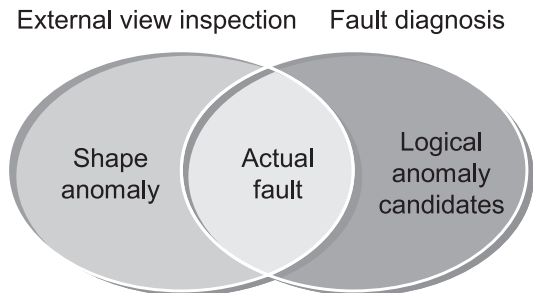


Fig. 3 Relationship between the shape anomaly and the logical anomaly candidates.

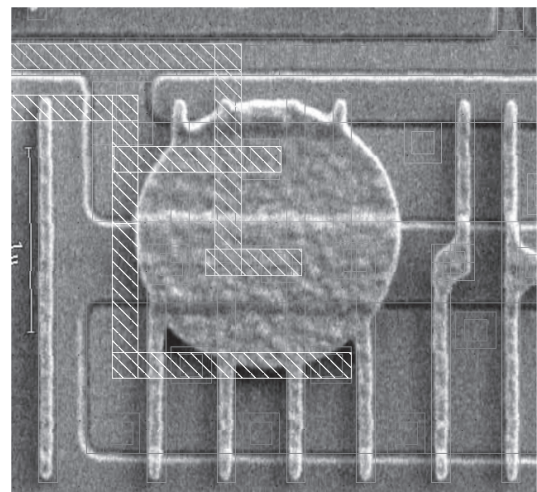


Fig. 4 Example of auto fault site identification (Hashed locations: Fault candidate obtained by fault diagnosis).

degree of influence of shape anomalies on the product yield. It is therefore very important to identify any shape anomalies that may lead to logic errors. However, this procedure requires analysis of a large number of samples and too much effort for FA engineers in the previous technique that had to identify the fault by sample.

To solve this problem, we have newly developed a technique for the automatic identification of critical shape anomalies leading to logic errors. This technique compares positions of the shape anomalies detected in the defect inspection process with those of fault candidates calculated by the fault diagnosis system, without physical failure analysis (Fig. 3 and Fig. 4). The fault diagnosis is capable of narrowing down the fault candidates at high speed and accuracy using technologies developed originally by NEC Electronics^{2), 3)}.

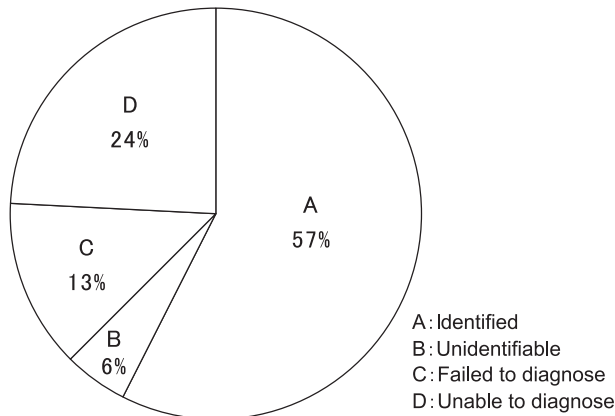


Fig. 5 Auto fault site identification rate.

Fig. 5 shows the fault site identification rate that is obtained by comparing the positions of the fault candidates of fault diagnosis and the shape anomaly detected with a defect inspection system. According to the figure, the technique has succeeded in the automatic identification of faults of 57% of the defective samples. The faults were not able to be identified in 6% of the samples because no shape anomaly was detected in the defect inspection process. Since there is a trade-off between the detection rate and the reduction in the number and time of inspections from the viewpoint of manufacturing TAT, it is difficult to eliminate the unmatched samples that fail to identify faults. Also, in the case of 13% of the samples, the fault diagnoses failed to locate the faults because they were complex multiple faults. In the case of 24% of the samples, fault diagnosis could not be performed because the test circuit block failed.

When the faults of a sample can be identified automatical-

Table Distribution chart of defective samples and suspected layers.

Sample	Open						Short							
	CT	M1	M2	M3	M4	M5	M6	CT	M1	M2	M3	M4	M5	M6
C1	o	o	o	o	o	o	o	o	o	o	o	o	o	o
C2				o	o	o								
C3				o	o	o								
C4				o	o	o								
C5	o	o	o	o	o	o	o	o	o	o	o	o	o	o
C6	o	o	o	o	o	o	o	o	o	o	o	o	o	o
C7	o	o	o	o	o	o	o	o	o	o	o	o	o	o
C8				o	o	o								
C9				o	o	o								
C10			o	o	o	o	o							
C11				o	o	o	o							
C12				o	o	o	o							
C13				o	o	o	o							
C14	o	o	o	o	o	o		o	o	o	o			
C15	o	o	o	o	o	o		o	o	o	o	o	o	o
C16							o	o	o	o				
C17							o							
C18			o	o	o	o								

(CT: Cell, M1-M6: Wiring layers)

(O: Fault candidate layer)

ly physical failure analysis using FA equipments is not required, so the time needed for the physical failure analysis can be reduced considerably from that of the previous method. In addition, if an image of the defect can be obtained, identification of the defective process and the type of defect makes it possible to decide the countermeasure quickly and feed it back promptly to the production line. On the other hand, the samples for which auto fault identification was not possible were subjected to physical failure analysis for the fault site identification.

3. Assumption of Defective Process and Identification of Fault Sites

The conventional fault isolation technique necessitates the use of advanced FA equipments to support PEM (Photo Emission microscopy), OBIRCH (Optical Beam Induced Resistance CHarge) or SDL (Soft Defect Localization), and takes

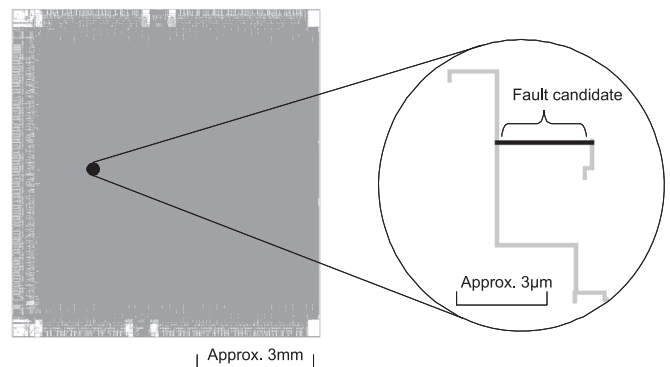


Fig. 6 Fault localization by fault diagnosis.

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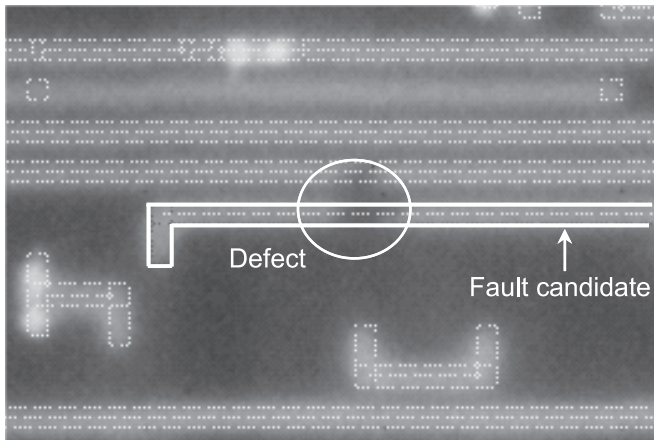


Fig. 7 Wiring layer of sample C3: M3 (Superimposed image of SEM micrograph and layout).

time to complete the isolation⁴⁾. However, the key to a timely improvement in yield is to quickly identify the causes of those faults that most affect the yield. For this purpose, we have newly developed a technique for efficiently isolating fault. This is achieved by estimating the defective process by diagnosis and by selecting samples to be subjected to physical failure analysis.

With regard to the fault diagnoses, we have developed a highly accurate technique for locating the faults at the level of a wiring section by making full use of design information (Fig. 6). This technique also totals the fault candidates on a per-wafer basis in order to find the suspected layer (the manufacturing process that may be failed) that is common to several defective samples. It also analyses layers and employs simplified physical analysis techniques with combination of surface grinding and observation in order to quickly isolate faults.

Table shows an example of the fault diagnosis summary of a wafer that have presented low yield in their lots. It shows that there may be open faults in wiring layer: M3 in 17 of the 18 samples. We therefore performed the grinding-and-observation technique to four samples C2, C3, C4 and C14. As a result, we found open faults in wiring layer M3, which is one of the fault candidates, in all of the four samples (Fig. 7). We fed back the result immediately to the production line and the countermeasures for preventing the open fault in wiring layer M3 were applied.

In this way, analyzing the layer distribution of fault candidates enables a rapid identification of faults by applying the simple analysis technique. However, this method cannot be applied to samples in which the faults cannot be localized by

means of fault diagnosis. Nevertheless, it is still possible to assume and extract the cause of faults on these fault localization failed samples, by analyzing samples from the same wafer for which a localizing the faults was successfully made. This is because there is a significant possibility that common faults exist on both types of samples. As a result of this procedure the new technique can be regarded as being more efficient than previous methods used for identifying the causes affecting the yield.

4. Conclusion

As described above, the time and cost involved in fault isolation may be significantly shortened by effectively utilizing the fault diagnosis technology for applying analyses aimed at supporting yield improvements. In the future, when the micro-fabrication and functional enhancements of LSIs are expected to advance as a result of the requirement for higher quality, the fault diagnosis technique that requires comprehensive technological capabilities will increase in importance compared to its current status. In order to meet this trend, we will promote the development of specific technologies aimed at enabling supportive diagnosis and analysis as well as by enabling their seamless connection.

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