Pioneering Development of Immersion Lithography

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Abstract

NEC Electronics has pioneered the development of the immersion lithography technology in order to deal with micro-fabrication from the 65nm logic to the 55nm logic and after. Instead of air, the immersion technology introduces water between the lens and wafer of the exposure system for use in fabricating the circuit pattern and this makes it possible to improve the resolution and to fabricate finer patterns than have been achieved hitherto. NEC Electronics has completed the material development, exposure system development and process optimization for this technology and the process is currently being applied to mass-production of the 300mm wafer production line at the NEC Semiconductors Yamagata factory.

Keywords

lithography, micro-fabrication, immersion, 55nm logic LSI, exposure, resist

1. Introduction

Micro-fabrication of LSIs has advanced steadily along with the evolution of the lithography technology process. The Rayleigh's equation shown below is often used to express the resolution of the lithography process.

Rayleigh's equation: Resolution = k1 · λ/NA

Where k1 = Process constant, λ = Exposure wavelength.

The resolution of an exposure system can be improved by decreasing the exposure wavelength and increasing the NA (Numerical Aperture) of the lens used. For this purpose, the light source used in the exposure for pattern formation has had its wavelength decreased from the g-line mercury lamp (wavelength = 436nm) to i-line mercury lamp (365nm), KrF excimer laser (248nm) and ArF excimer laser (193nm). The NA has also been increased thanks to the fabrication technology and an exposure system with an NA at the almost limit value of 0.9 or more has already been implemented. The 90nm and 65nm logic LSIs presently mass-produced use the ArF lithography that adopts an ArF excimer laser as its light source. With the present research, NEC Electronics has developed and introduced immersion lithography as the next-generation ArF lithography for the implementation of finer LSIs such as the 55nm logic LSI.

2. Immersion Lithography

Immersion lithography performs the exposure process by filling the space between the lens and wafer of the exposure system with liquid as shown in the right half of **Fig. 1** . The presently practiced immersion lithography is the ArF immersion lithography process that uses an ArF excimer laser as its light source and water as the immersion liquid filled between the laser and wafer. The ArF excimer laser beam used as the exposure light has a refractive index *n* of 1.44 with water, so

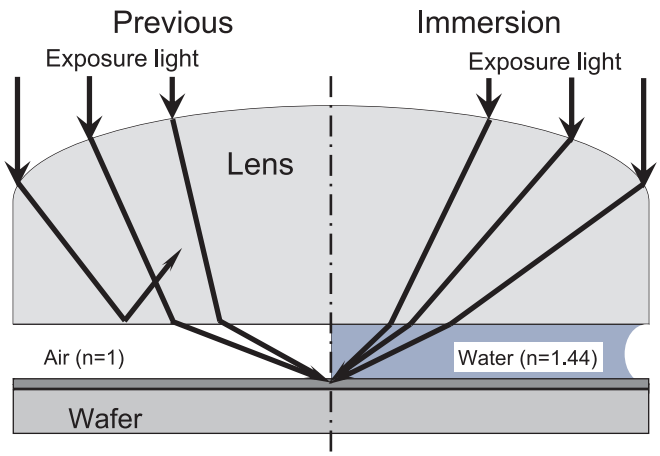

Fig. 1 Concept of immersion lithography.

the angle of the exposure light incident on the wafer is smaller than for air (n = 1). This makes it possible to increase the NA over 1 and to improve the resolution. Even when the same NA as before is used in the exposure, the small wafer incidence angle makes it possible to increase the depth of focus (the range at which the light is focused enough to form a pattern) by about 40% and to thus assure a stable yield. At present an exposure system incorporating a lens with a high NA of max. 1.35 using water immersion exposure is already available.

As immersion lithography requires the introduction of water for exposures that used to be processed in air, we encountered a large number of issues including those related to the resist process and the exposure system in our efforts for practical implementation. Below we describe our development efforts.

2.1 Development of an Immersion Compatible Resist Process

There has been a lot of concern related to pattern formation by means of immersion lithography, such as the defective pattern shapes due to water penetration in the resist film that was caused by the leaching of various resist film constituents into the water and the consequent pattern defects derived from the leached impurities or from foreign objects inside the exposure system. In addition, as any water droplets remaining on the wafer after immersion exposure will also cause a pattern defect, it is necessary to completely eliminate water after exposure, as well as to render the resist film surface hydrophobic during exposure. Therefore, with the newly developed immersion resist process that features 55nm node compatibility, we have applied an immersion topcoat film in order to ensure the hydrophobic property as well as for protecting the surface to the ArF resist process for the 65nm logic LSIs [1,2] . **Fig. 2** shows the immersion exposure process. The topcoat film is applied on the traditional resist film as shown in Fig. 2(a), then exposure is performed with an exposure system in which immersion water is filled between the lens and wafer as shown in Fig. 2(b), and the resist pattern as shown in Fig. 2(c) is formed after the exposure. Later, the topcoat film is peeled off and removed by the alkaline development solution during the development process.

When introducing the topcoat, we evaluated the suitability of various topcoat films to the resist used with the 65nm logic LSIs. Some examples of the results of SEM (Scanning Electron Microscopic) observations of cross-sectional shapes of resist patterns after development [1] are shown in **Fig. 3** . Fig.

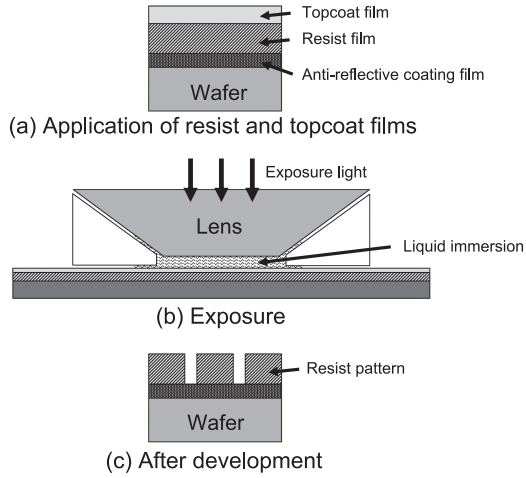

Fig. 2 Immersion-compatible resist process.

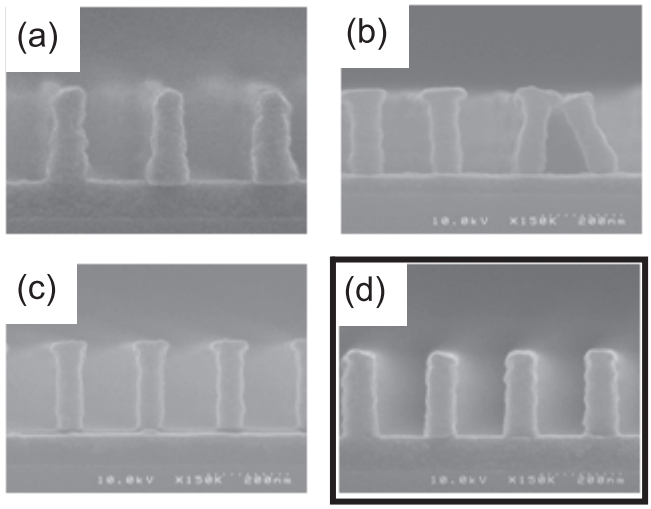

Fig. 3 Results of immersion-compatible topcoat evaluation.

3(a) to (d) are observations obtained by forming the patterns by combining four different topcoat films to the same resist. As (a) presented rounding on the upper part of the forward tapered shape, (b) and (c) presented projections on the upper part accompanied with side toppling and/or shape deterioration and (d) presented a satisfactory pattern shape. Therefore, we decided to adopt topcoat film (d) in our immersion resist process.

Introduction of the topcoat has made it possible to protect the resist film during immersion exposure as shown in Fig. 2(b) and to thus prevent penetration of water and leaching of various resist film constituents into the water. At the same time, we

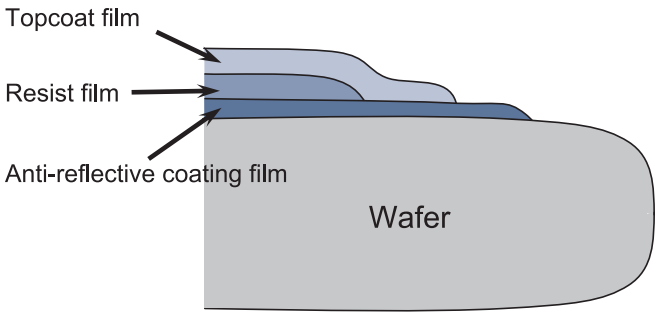

Fig. 4 Film structure at the wafer edge.

also succeeded in securing the hydrophobic property of the surface, retaining the liquid immersion only in the exposed area between the lens and wafer of the exposure system, and preventing water droplets from remaining on the wafer after exposure.

On the other hand, we also found that the immersion-compatible topcoat has a poor adhesion with the wafer. Particularly, if the topcoat film is formed with direct coating on the edge section of the wafer, the film is peeled off easily under immersion exposure. Any of the topcoat thus peeled off and into the immersion liquid may screen the exposure light during exposure and cause pattern defects. When we evaluated the adhesion of the topcoat film, we found that the topcoat film has good adhesion with the resist film and the anti-reflective coating films [3], and decided therefore to form the topcoat film only on the anti-reflective coating film as shown in **Fig. 4** . This structure has made it possible to avoid the topcoat film peeling at the wafer edge.

2.2 Development of an Immersion–Compatible Exposure System

For the method of filling the space between the lens and wafer with water, we adopted the partial fill method that introduces water immersion only partially in the surroundings of the exposure area between the lens and wafer. We also applied measures to ensure that water would not remain on the wafer after completion of exposure. Some of the possible problems with the immersion exposure system are deterioration of the overlay accuracy and defocusing during exposure, which may be caused by expansion, contraction or deformation of water due to the temperature fluctuations resulting from the contact of water with the wafer. In order to prevent these problems, various measures are taken for example by controlling the

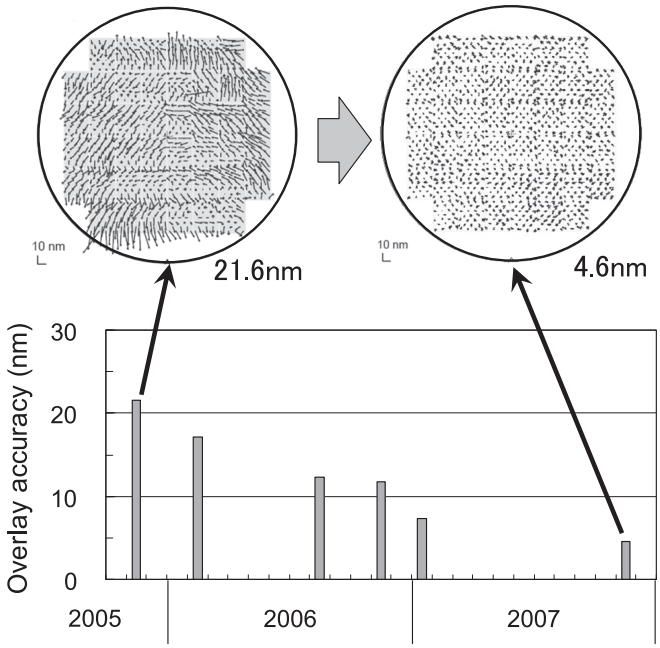

Fig. 5 Improvement of overlay accuracy of immersion exposure system.

immersion water temperature with very high accuracy and by providing the wafer-holding stage with a temperature control function for preventing changes in the water temperature. As seen in **Fig. 5** , the immersion exposure system introduced in the initial stage of development in 2005 was not capable of sufficient temperature control and optimization and the overlay accuracy derived from the exposure system alone was as poor as over 20nm, which was not sufficient for the required accuracy of 12nm [4] . This problem was particularly noticeable for the peripheral area of the wafer as indicated by the position error vector shown in the wafer map above the graph. By 2007, however, we eventually succeeded in improving the accuracy to below 10nm thanks to various measures and optimization efforts.

2.3 Application of Immersion Lithography to 55nm Logic LSI

Fig. 6 shows the results of pattern formation achieved by applying the immersion resist process and immersion exposure system discussed above to the processes of the 55nm logic LSI [3,4] . The figure shows that the formed pattern has

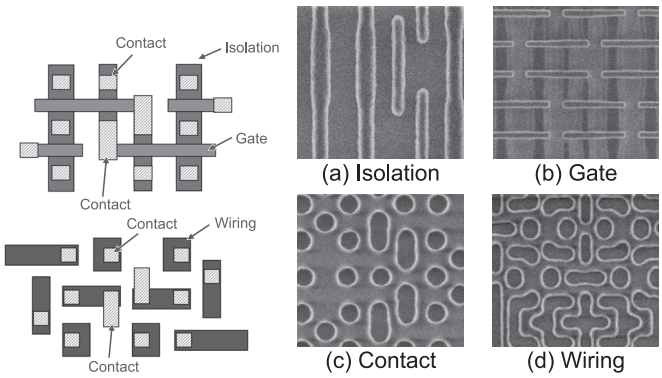

Fig. 6 55nm logic LSI pattern using immersion lithography.

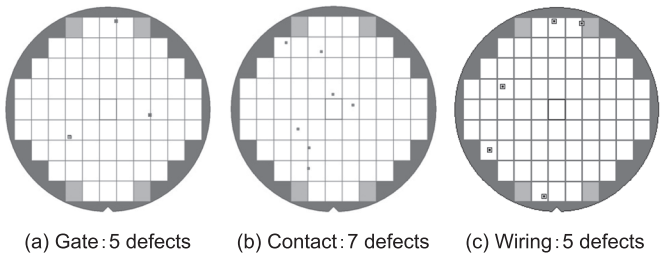

Fig. 7 Pattern defects in immersion lithography.

achieved a very good shape. The overlay accuracy at the 25nm level is required for the 55nm logic LSI, and we confirmed that we had been successful in satisfactorily achieving the desired accuracy by applying the newly developed immersion lithography to actual LSI process wafers [4].

We also evaluated the pattern defect (which is a source of problems in immersion lithography) with the patterns obtained in actual 55nm logic LSI fabrication processes and confirmed that the level is equivalent to or better than that of the previous lithography process. **Fig. 7** shows an example of the results of defect inspections of patterns formed on the entire surface of a 300mm wafer by means of immersion lithography. The number of defects was below 10 in any of the processes.

The immersion lithography technology described in the above is currently being applied to the mass-production process of 55nm logic LSIs at the 300mm wafer fabrication line at the NEC Semiconductor Yamagata factory.

2.4 The Future of Immersion Lithography Technology

The immersion lithography has been developed for the 55nm logic LSIs and is already introduced in the mass-production process. It is currently used also in the development of 40nm and 32nm logic LSIs and we also plan to apply it in the production of these LSIs. At present, with the aim of cost reduction, we are developing a resist equipped with the topcoat function. When implemented practically, it is expected that this resist will make the currently used topcoat unnecessary. With the 32nm logic LSI, we expect that we will be able to use a system capable of achieving an NA of 1.35, which corresponds to the highest level possible with the current immersion lithography process using water. Furthermore, we are also developing lithography technologies that feature compatibility with the next-generation LSIs that will follow the present development. These will include the double patterning technology that overlaps exposure and pattern formation by repeating immersion exposure and the EUV (Extreme Ultraviolet) lithography that uses UV light with the very short wavelength of 13.5nm. Both of these are extremely difficult processes to implement and we are encountering many problems for their implementation at the present time. The double patterning technology using repeated exposures is a technology aiming at prolonging the life of immersion lithography, but it also poses very difficult problems such as an overlay accuracy requirement of 2 to 3nm. We are currently developing the requisite element technologies to support this technology.

3. Conclusion

We have succeeded in implementing an immersion lithography that is to be the next-generation micro-fabrication technology to succeed the ArF lithography process. This has been achieved by developing and optimizing the topcoat process and an immersion exposure system. At present, the developed technology is being applied in the fabrication of 300mm wafers at the NEC Semiconductors Yamagata factory as the exposure technology for the 55nm logic LSI and it is scheduled for application to the 40nm logic LSI in the near future.

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References

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