40nm Node CMOS Platform “UX8”

FUKAI Toshinori, IKEDA Masahiro, TAKAHASHI Toshifumi, NATSUME Hidetaka

Abstract

The UX8 is the latest process from NEC Electronics. It uses the most advanced exposure technology to achieve twice the gate density of the previous generation. It adopts new technologies to improve performance, as well as to enable embedding of memories, including SRAM and DRAM, in core, 1.8V and 3.3V type transistors. In addition, the UX8 is implemented as a device platform for a wide range of users who may use it in logic products, as well as DRAM-embedded products, because it offers a selection of two kinds of core devices, including the 0.9V LOP (Low Operation Power) and 1.1V LSTP (Low STandby Power) cores, which can deal with applications ranging from those featuring high-speed operation to those featuring low power consumption. This paper is intended to introduce the representative technologies applied in the UX8 and its device lineup.

Keywords

LSI, low power consumption, embedded memory, SRAM, DRAM

1. Introduction

We have developed a series of 40nm node CMOS platforms (code name: UX8) that can implement system LSIs featuring large-scale integration, low power consumption and low cost.

With the UX8, the core transistor has a gate length of 40nm and gate insulation film thickness of less than 2.0nm. The lithography process used to form such a fine pattern is the most advanced immersion exposure. The gate insulation film of the UX8 is made of a high-k material (Hf-doped silicate) that has been applied to a 55nm node (UX7LS) for the first time in the world to ensure the high performance of the transistor.

Table shows the change of technologies used by NEC Electronics from the 90nm node (UX6) to the UX8.

The UX8 achieves performance improvement by brushing up the power consumption reduction technologies we have cultivated, while avoiding an increase in manufacturing costs by adding a minimum number of new technologies. From the initial stage of development, we conducted the development assuming embedding of DRAM in order to provide the UX8 with device platforms meeting the needs of a wide range of users, including those who apply it in most advanced memory-embedded logic products.

This paper introduces the new technologies adopted by the UX8 as well as its device lineup.

Table Summary of key technologies.

process Name	UX6M/H	UX7LS	UX8L/G
Node(nm)	90nm	55nm	40nm
Lg(nm)	60nm	50nm	40nm
gete dielectric	SiON	Hf-doped silicate	Hf-doped silicate
channel direction	<110>	<100>	<100>
activation tool	RTA	RTA	MSA
Silicide	CoSi	NiSi	NiSi
Litho. tool	ArF Dry	ArF wet	ArF wet

2. UX8 Platform Suitable for Large–Scale Integration

In general, the shrinking rate (of the transistor pitch or interconnect pitch) in the X-axis (or Y-axis) direction is equal to 0.7X, according to Moore’s Law. When this is converted into area, the shrinking rate is $0.7 \times 0.7 \approx 0.5$, which means that advancement by one generation makes it possible to implement the functions of the previous generation in half the area of a semiconductor chip. At NEC Electronics, we adopted the most advanced immersion system at a very early stage (for details, see “Pioneering Development of Immersion Lithography” on pages 58 to 62 of the present issue), and, with the core transistor of the UX8, we succeeded in achieving a minimum gate length of 40nm and twice the gate density of the previous generation (up to 2,000k Gate/mm ^{2}) (**Fig. 1**).

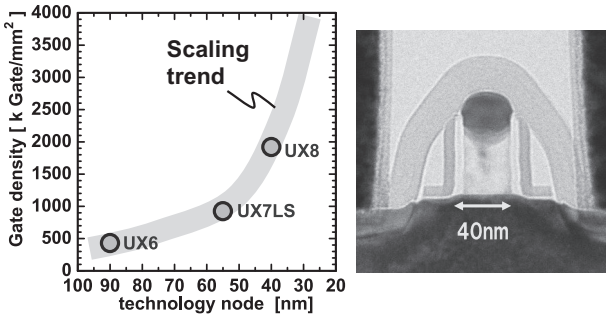


Fig. 1 Gate density trend and cross-sectional TEM image.

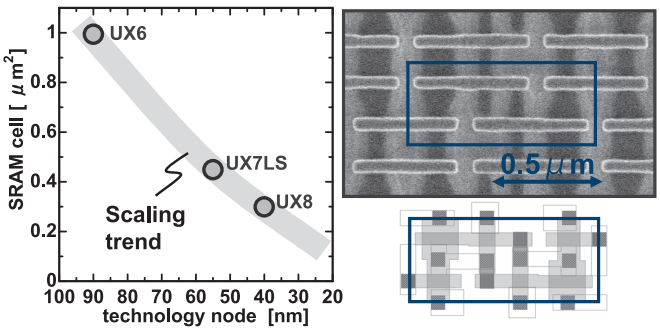


Fig. 2 SRAM area trend per cell, and bird view SEM Image after gate electrode formation.

We also succeeded in stable implementation of an SRAM that is suitable for large-scale integration, thanks to a cell area of less than 0.3μm [2] (**Fig. 2**).

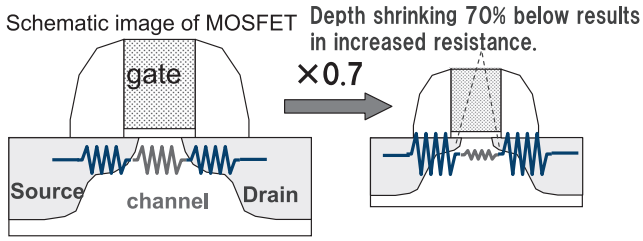
3. High–Performance UX8 Transistor Technology

The performance of a transistor cannot be improved by simply shrinking the design discussed above. This is because there are factors that cannot be scaled. In this section, we will describe the technologies we utilized to overcome these unscalable factors.

3.1 Technology for Transistor Size Reduction

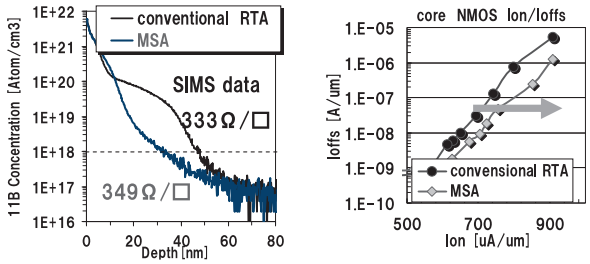
- Application of MSA (Milli-Second Annealing)

To obtain stable transistor characteristics with small gate length L, it is necessary to reduce the distribution of



Scaling reduces channel resistance (which is good), but transistor performance deteriorates because source/drain depth must be reduced more than the scaling ratio to suppress short channel effect.

Fig. 3 Issue in shallow junction of SD extension.



MSA processing makes it possible to implement equivalent resistance to conventional RTA with a 2/3 junction length compared to the conventional design.

MSA processing improves the I_{on} current characteristic.

Fig. 4 Improvement in sheet resistance and Transistor Ion thanks to MSA.

impurities [*1] in the source/drain (SD). On the other hand, as the activation rate of impurities introduced in the SD region is already nearly saturated, simply making the SD shallow increases the SD resistance, and causes the problem of transistor current drivability degradation (**Fig. 3**).

The thermal process traditionally used to activate SD impurities has been the RTA (Rapid Thermal Annealing) process, which applies thermal treatment for one second to several tens of seconds in a temperature range of 1,000 to 1,100°C. With this process, when the thermal treatment temperature is increased to get lower resistance, the impurities are diffused and the junction becomes deep.

To solve this problem of the previous technology, we applied the MSA process to the UX8. The MSA is an annealing process that performs thermal treatment at 1,200 to 1,300°C for a millisecond (1/1,000 sec.), and can achieve a high impurity activation rate without causing diffusion of impurities.

[*1] “Impurities” refers to the electrically active elements introduced in silicon. They are generally arsenic and phosphor with the N-type, and polonium and indium with the P-type.

Fig. 4 shows the relationship between junction depth and the resistance of the impurity diffusion layer. Here, we can see that the MSA makes possible a shallow junction and low resistance thanks to high-rate activation of impurities. The effects of MSA are expressed in transistor characteristics, and higher ON current (I_{on}) than the previous RTA process can be obtained from the same OFF current (I_{off}).

3.2 Technology Enabling Stable Circuit Operation Even under Low Supply Voltage

-Application of Hf-Doped Silicate

At NEC Electronics, we have been applying an ultratrace amount of Hf-doped silicate in the gate insulator film (**Fig. 5**) since the UX7LS to lower the channel impurity concentration of transistors.

A low channel impurity concentration brings about three advantages in the transistor design. The first advantage is a reduction of the leak current between the drain and the substrate, and the second is a lightening of the effects of currier scattering and an improvement in mobility μ_{eff} (**Fig. 6**).

Finally, the third advantage of a low channel impurity concentration is a reduction in the random variations of transistor characteristics. When the device size is scaled down to less than 0.1μm, the number of impurity atoms in the channel region of a transistor to a number that can almost be counted one by one. Therefore, random variation between transistors, due to statistical fluctuations in the number of impurity atoms, has recently become a new problem.

Fig. 7 shows the current variations at nodes A and B of an SRAM. The figure shows that random variations in the transistors used in the SRAM make the relations between nodes random, but that the random variations are smaller with the device applying Hf-doped silicate.

The effects of fluctuations in the number of impurity atoms are dependent on transistor size, increasing at a rate of $1/\sqrt{LW}$ (where L represents gate length and W gate width), causing one of the problems hindering scaling. This problem increases the difficulty of circuit design (as shown by the line extending from the conventional technology toward the 40nm node in **Fig. 8**), because variation increases by $1/\sqrt{LW} = 1/\sqrt{0.5} = 1.4X$ per generation, and the number of transistors mounted per unit area on a chip doubles, and variation width increases simply. At NEC Electronics, we succeeded in alleviating the burden on circuit design due to scaling by reducing random variations by means of device optimization using Hf-doped silicate (as shown by the line for trace Hf in Fig. 8).

For example, the effects of a reduction in random variations are most noticeable in the SRAM yield. The Hf-doped silicate also made it possible to reduce the minimum operation voltage (**Fig. 9**).

As described above, Hf-doped silicate gate insulation film has not only improved transistor performance, but has also

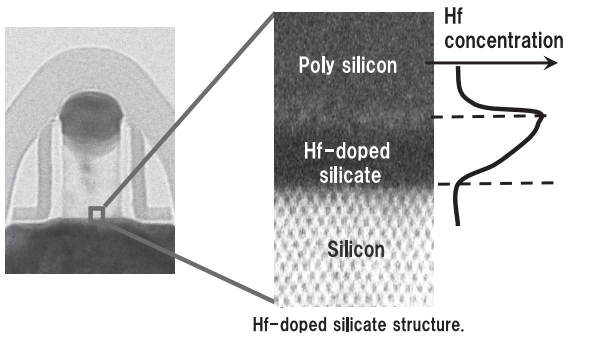


Fig. 5 Cross-sectional TEM images of a transistor and Its Hf-doped silicate structure.

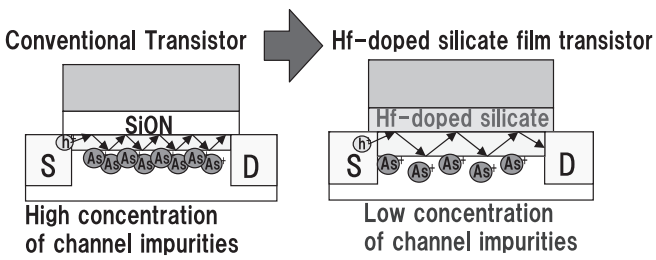


Fig. 6 Advantages of a transistor using Hf-doped silicate.

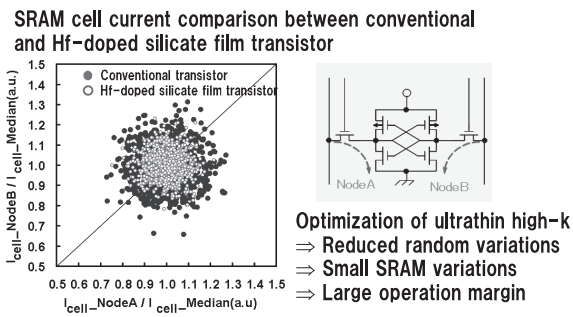


Fig. 7 Effect of random variation reduction.

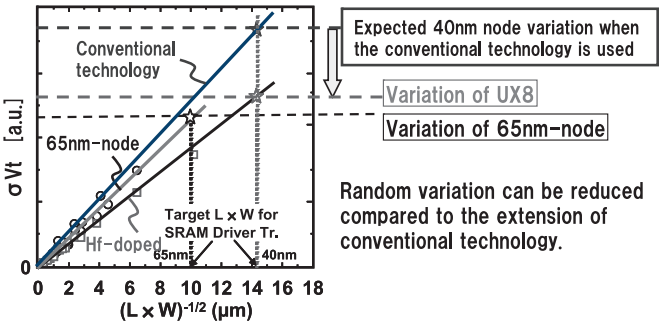


Fig. 8 Transistor sizes and random variations.

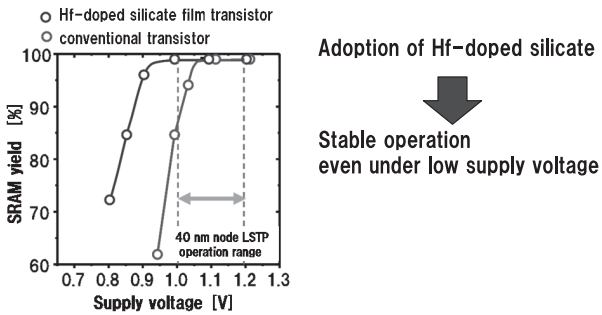


Fig. 9 Supply voltage dependence of SRAM yield.

enabled stable circuit operation with a lower supply voltage.

4. UX8 Device Lineup

For the UX8, we developed two kinds of core devices, including the 0.9V LOP (Low Operation Power) device featuring low active power and the 1.1V LSTP (Low STandby Power) device featuring low standby power, creating a CMOS platform allowing users to select the core device according to their specific requirements for LSI power consumption reduction. In addition, we advanced the development assuming DRAM embedding from the initial stage, and prepared the process targeting the most advanced memory-embedded logic products. **Fig. 10** shows the cross-section of the DRAM section of a memory-embedded logic circuit. DRAM embedding can be fabricated by inserting an additional process for forming memory capacity between the substrate process and the first-layer interconnect process of the CMOS process.

The advantages of embedded DRAM include a 1/4 cell-area reduction compared with SRAM as well as great reductions in

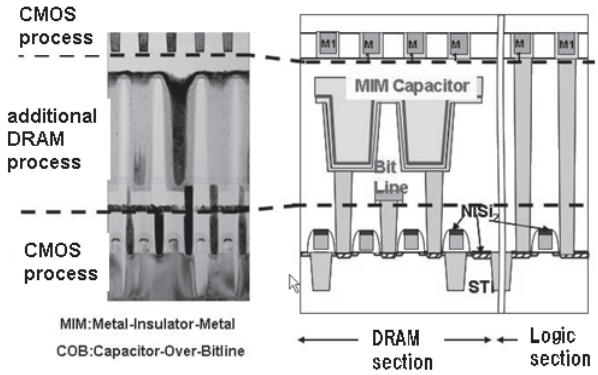


Fig. 10 Cross-sectional structure of DRAM capacitance section of embedded DRAM process.

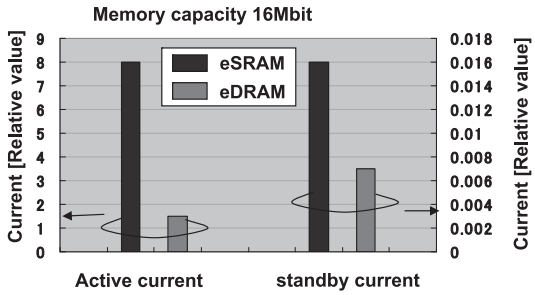


Fig. 11 Advantages of embedded DRAM (Power consumption reduction).

active power and standby power, as shown in **Fig. 11** . The embedded DRAM is therefore suitable for reducing the power consumption of an SOC with a large-capacity embedded memory.

5. Conclusion

We developed a 40nm node CMOS platform "UX8" offering twice the gate density of the previous generation. We implemented the UX8 as a high-performance device by brushing up the power consumption reduction technologies we have cultivated, while avoiding an increase in manufacturing costs by adding a minimum number of new technologies. At NEC Electronics, we are determined to offer system LSIs that can achieve low power consumption and high speed with a wide range of applications using the UX8 process.

Authors' Profiles

FUKAI Toshinori
Senior Process Engineer,
Advanced CMOS Technology Group,
Advanced Device Development Division,
NEC Electronics Corporation

IKEDA Masahiro
Senior Expert,
Advanced CMOS Technology Group,
Advanced Device Development Division,
NEC Electronics Corporation

TAKAHASHI Toshifumi
Team Manager,
Memory Device Development Group,
Advanced Device Development Division,
NEC Electronics Corporation

NATSUME Hidetaka
Team Manager,
Memory Device Development Group,
Advanced Device Development Division,
NEC Electronics Corporation