Packaging Technology of the SX-9

UMEZAWA Kazuhiko, HAMAGUCHI Hiroyuki, TAKEDA Tsutomu
HOSAKA Tadao, NATORI Masaki, NAGATA Tetsuya

Abstract

This paper is intended to outline the packaging technology used with the SX-9. With the aim of enabling the CPUs implemented with the world's highest single core performance to exhibit their maximum performances; the SX-9 makes full use of high-density LSI packaging technology, high-density connection technology, high-efficiency packaging technology and high-performance power supply technology. These technologies are packaged with the aim of achieving an excellent system effective performance with a wide memory bandwidth of 4T bytes/sec. per node. The SX-9 adopts an advanced design in order to appeal its high performances both of the processors and the system to the users.

Keywords

packaging technology, board, packaging, connection, cabinet, power supply, design

1. Introduction

What is most characteristic of the Supercomputer SX Series is that all of the CPUs share all of the memory space within a node (shared memory system). In order to utilize the entire shared memory system efficiently, we pursued optimization of the whole of the SX-9's packaging structure as required for high speeds in LSI operation and chip-to-chip interconnection. We succeeded thus in achieving high-density, high-efficiency packaging. In the following sections, we will introduce the SX-9's packaging technology that has been developed in order to achieve the above optimization.

2. High–density Packaging Technology

CPU and RTR interposer (RTR-IP) packages are required for operations at ultra-high speeds. Consequently we have developed high-I/O-count LSI by further advancing the high-density packaging used with the SX-8 and have incorporated it in the SX-9. **Photo 1** and **Photo 2** show external views of the CPU and RTR-IP packages respectively. With regard to the CPU package, the CPU LSI is mounted in the form of a bare die on the surface of a large build-up PWB, and a high-density multi-terminal connector is mounted at the back side. With the RTR-IP package, the RTR LSI is mounted on the front side of a glass-ceramic substrate and the solder balls for connection to the RTR board are formed on the back side. The RTR-IP is packaged in the RTR module, which is a mother card,

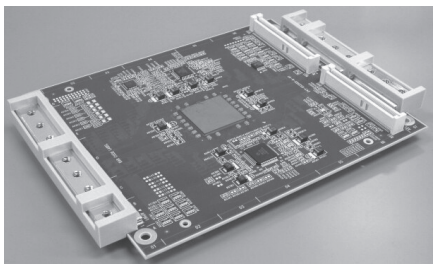

Photo 1 CPU package.

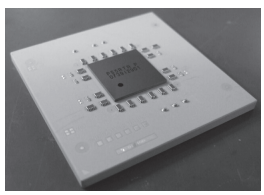

Photo 2 RTR-IP package.

together with the MMU module. **Table 1** shows the specifications for the CPU package, the RTR-IP package and the MMU module.

2.1 LSI Packaging Technology

In order to let the LSIs exhibit maximum performance we have adopted bare die packaging compared to the SX-8 that features an increased density. The CPU LSI is connected to an ultra high density build-up PWB and the RTR LSI to a glass-ceramic substrate, both using lead-free solder. The reliability

Table 1 CPU/RTR-IP/MMU module specifications.

Item		CPU	RTR-IP	MMU module
LSI (Form)		CPU LSI×1 (Bare die)	RTR LSI×1 (Bare die)	HUB LSI×1 (BGA) DRAM ×24 (BGA)
	Number/Pitch of pins	8960/168μm	6093/168μm	840/1.0mm
	Size(mm)	19.84×21.04	15.98×15.98	31×31 ※HUB LSI
Wiring board	Type	Build-up PWB	Glass-Ceramic substrate	PWB
	Size(mm)	140(W)×112.5(D)×1.6(t)	50(W)×50(D)×3.4(t)	65(W)×135(D)×1.6(t)
	Number of layers	4 builds-8 cores-4 builds	35	12
	Wiring density (μm)	Line/Space =18/18	Line/Space =66/60	Line/Space =80/80
Number of package terminals		2,628	3,600	170

Table 2 RTR module board specifications.

Item	RTR Module Board
Size(mm)	310(W)×294(D)×4.5(t)
Material	Low Dk/Df material
Number of layers	28 (including 9 signal layers)
Wiring density	2 traces / 0.8 mm
Wiring specifications(μm)	Line / Space =65 / 70
Packaged devices	CPU Connector×17,RTR-IP×2, MMU module×32

of the connections between the LSIs and the wiring boards is ensured by the under-fill resin. Improved fabrication technologies including the fine pitch soldering, mounting and resin filling have increased the number of connection terminals and reduced the pitch compared to the SX-8.

2.2 Wiring Board Technology

1) Ultra-high Density Build-up PWB

The build-up PWB used with the CPU package features micro-fabrication with a wiring pitch of 36μm (line and space = 18/18μm) adopts to the fine line formation using the semi-additive process and the micro-via formation by the laser process. Four build-up layers are fabricated both on the front and back sides to enable fanout of all the signals by connecting more than 8,000 C4 bumps of bare die.

2) High/Multi-layer Printed Wiring Board

The RTR module board is a multi-layer PWB made of the most advanced materials and featuring excellent electrical properties (relative dielectric constant of 3.7 and dielectric loss tangent of 0.002). The components are placed to a high density in order to reduce the wiring length, and measures to enable high-frequency signal transmission are taken, including optimization of the component pad shapes, adoption of a structure with reduced through hole capacitance and use of low-profile copper foil with reduced surface roughness. The pin assignments of each component are also optimized and the wiring capacity is improved by routing between the 0.8mm-pitch through holes with a line and space of 65/70μm. **Table 2** shows the specifications of this PWB.

3. System Packaging Technology

Fig. 1 shows the system configuration, which is a shared memory configuration in which all of the CPUs are connected to all of the MMUs via RTRs. We adopted the 4 sides mounting method as shown in **Fig. 2** in order to efficiently connect the modules composing the shared memory system. This method mounts 16 CPU modules on both the front and

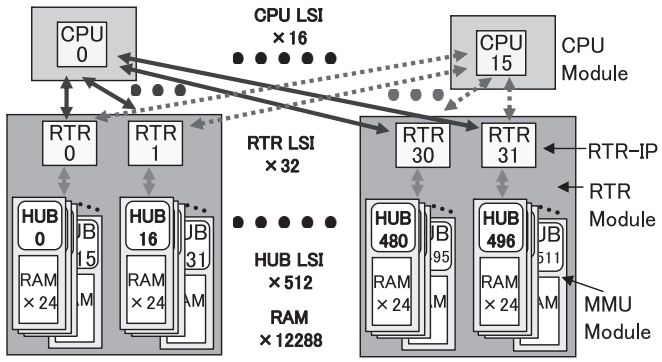

Fig. 1 SX-9 system configuration (Packaging layer diagram).

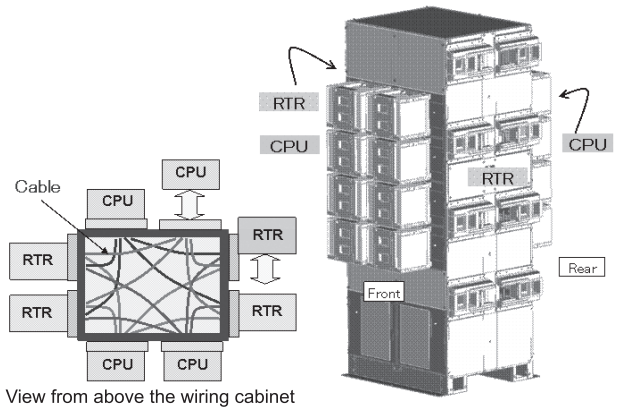

Fig. 2 Packaging structure diagram.

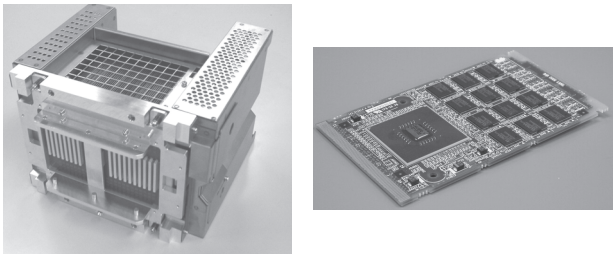

Photo 3 CPU module and MMU module.

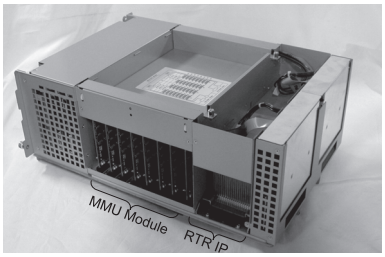

Photo 4 RTR module.

back sides of the wiring cabinet which is accomodating cables and 16 RTR modules on both the left and right sides. It also connects the above modules directly using 256 high-frequency multi-core cables to implement ultra-high-speed interfacing between each of the LSIs. Thus, it achieves a performance of 1.6TFLOPS per node and a memory structure sharing 1T bytes. We also enabled either side maintenance despite 4 sides mounting, by mounting the RTR modules so that they can be serviced from the same directions as the CPU modules.

3.1 Packaging of the CPU/MMU/RTR Modules

Photo 3 and **Photo 4** respectively show external views of the CPU, MMU and RTR modules. The CPU module includes the CPU package, optical module and DC-DC converter plus the cable connectors at the back side. The MMU module includes the HUB LSI and the RAMs. The RTR module includes the RTR-IPs and MMU modules plus the cable connectors at the back side.

3.2 Connection Technology

We developed a high-frequency multi-core cable and a cable insertion mechanism to implement high-speed interfacing between the CPU and RTR modules (**Photo 5**).

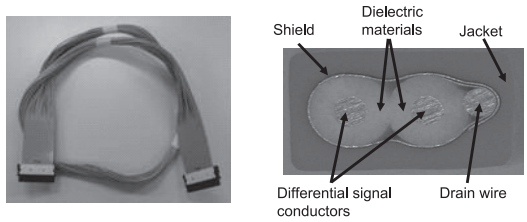

Photo 5 High-frequency multi-core cable and wire cross-section.

(1) High-frequency Multi-core Cable

Side-drain type micro Twinax cables are used that have EPTFE as the dielectric material in order to achieve a high-density transmission of high frequency. This has made possible a contact pitch of 0.5mm and implements high-density connections by accommodating 48 channels of differential signals (146 pins) in an occupation area of 225mm ^{2} on the PWB.

(2) Cable Insertion Mechanism (Cable Connection Mechanism)

To enable the efficient connection of about 600 cables (18 per CPU module, 17 per RTR module) in a node, we adopted connections using cable insertion mechanisms. This technology had been developed for the previous SX Series and a single operation allows multiple cables to be connected simultaneously.

4. Cabinet Technology

For the SX-9 Series we adopted a cabinet structure that emphasizes the performance. The cables interconnecting the modules are routed via the wiring cabinet at the center of the CPU cabinet and the CPU and RTR modules are mounted efficiently around it in order to achieve high density packaging. Nevertheless, this has led to a concentration of unit heat sources and it has thus become an important issue to cool them efficiently. We have solved this problem and have made it possible to install the system easily in an ordinary machine room without the addition of special facilities. This has been achieved by improving the cooling efficiency using simulations and by actual machine evaluations in order to optimize the cooling air distribution and flow direction according to the amount of heat generation of each component.

5. Power Supply Technology

In order to improve the installation area and power consumption of the SX-9, we have decreased the size and increased the efficiency of the power supply system with high-density packaging. We have adopted a 48V DC power supply system, which inputs 200-240V AC to the AC-DC converters and distributes 48V DC to the DC-DC converters. Multiple AC-DC converters are operated concurrently at the front end to supply power according to the scale of the system configuration. In order to enable system operation even when an AC-DC converter fails, N+1 redundancy is used to reserve reliability. The reliability is further improved by duplication of the AC input. The DC-DC converter converts 48V DC into a 1.0-3.0V DC. Since it is required to reduce voltage drop in the power supply system and fluctuations of voltages due to load variations in order to supply a large current near to 200A at the low voltage of 1.0V, we have reduced the power supply impedance and inductance by connecting a DC-DC converter directly to the CPU and the RTR modules via busses or connectors.

Photo 6 shows the external view of the DC-DC converter developed for the SX-9. The input voltage is 48V DC, the output voltage is 1.0-3.3V DC and the output current is max. 260A. The size of the PWB is 140mm × 150mm, a component height is about 20mm, packaging density of 620A/liter, which is about 170% of the packaging density of the previous SX-8. The power efficiency peaks at 85%, which is a relatively high value for such a low-voltage and large-current DC-DC converter.

6. Design

We have designed the Supercomputer SX Series by setting "Evolution & Innovation" as the main concepts.

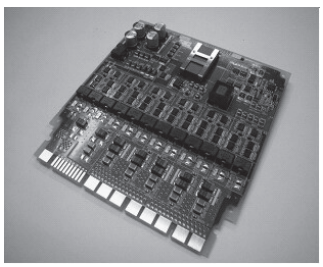

Photo 6 DC-DC converter.

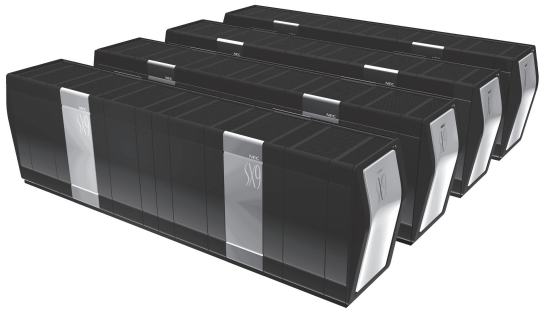

Photo 7 Overall view of the Supercomputer SX-9.

In designing the new SX-9, we inherited the main concepts above but attempted to express a new supercomputer image by tackling three major design challenges (**Photo 7**).

(1) Smart, Advanced Shape

The SX-9 end covers featuring complex curves are the result of a hybrid configuration of sheet metal and molds. Above all, the frame features both attractiveness and high workability by adopting the advanced press processing technology. The overall formative design is intentionally made simple in order to make the end panels stand out.

(2) Transmitted-light Logo Design Using High-intensity LEDs

The "X" in the SX-9 logo on the end covers uses a transmitted illumination character as the symbol of the new design. In addition, in order to distinguish the new SX-9 from the stationary design of the previous SX Series, the logo flashes gently every few seconds to offer an active image involving both time and spatial axes.

(3) High-quality, Gross-finish in Black

The overall coating of the SX-9 uses a black paint with attractive, obsidian like gloss, which enhances the value of the product. In the past, use of gloss paint has been possible only for limited products such as automobiles produced at large mass-production facilities. However, we have enabled its use for supercomputers by various studies and efforts, including the installation of a clean room in the paint workshop.

In addition to the styling features as described above, we have also applied measures to support a flexible layout and have cleared various conditions in order to provide the SX-9 with a design that has high appeal that is balanced to a higher than usual degree.

7. Conclusion

In the above, we introduced the packaging technologies and design concepts of the SX-9. We would also like to mention that the SX-9 is an environmental consideration computer product that complies with the environmental consideration standards and green procurement regulations set by NEC.

We believe that the contribution to the society through the development of the supercomputers which has the high performance, high reliability and cost efficiency is the mission imposed on us at NEC. In the future, we intend to contribute to the development of more attractive products by endeavoring to achieve further improvements in our packaging technologies.

Authors' Profiles

UMEZAWA Kazuhiko
Chief Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

HAMAGUCHI Hiroyuki
Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

TAKEDA Tsutomu
Assistant Manager,
Computers Division,
1st Computers Operations Unit,
NEC Corporation

HOSAKA Tadao
Expert,
Computer Common Technology Dept.,
NEC Computertechno, Ltd.

NATORI Masaki
Expert,
Computer Common Technology Dept.,
NEC Computertechno, Ltd.

NAGATA Tetsuya
Expert Designer,
Second Product Design Dept.,
NEC Design, Ltd.