Compact/Slim Proadlizer

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Abstract

The Proadlizer is a decoupling device that absorbs noise over a wide frequency range up to the gigahertz band and stabilizes the power supply line by quickly supplying it with current. This paper is intended to introduce the D-Case products (9.5mm × 5.5mm × 2.2mm), which are new products featuring a compact and slim design and the downsizing of the F-Case products (9.5mm × 12.1mm × 2.5mm) that were introduced in the NEC Technical Journal last year. These products also feature a test board mounting an FPGA (Field Programmable Gate Array) that is being adopted for network and broadcasting devices.

Keywords

compact, slim, noise suppression, transmission line, power supply isolation

1. Introduction

Recent trends in the electronics market are characterized by the progress of multi-code chips, decreases in voltages and increases in frequencies. These trends in chip usage also make it an urgent consideration for passive components such as capacitors to be decreased in size in order to support an increased number of functions and to reduce the number of their component parts.

Against this background, we at NEC TOKIN have succeeded in the successful mass production of the Proadlizer, which is a new decoupling device that features both an excellent decoupling function and a noise prevention function with low impedance over a wide frequency band and a large capacitance.

This paper describes the Proadlizer that has now begun to be mass-produced as well as other compact/slim Proadlizer products that are expected to further expand the market.

2. Outline of the Proadlizer

The Proadlizer has an aluminum anode and a conductive polymer cathode. It forms a stripline type structure that is the usual technology for use with high frequencies and it maintains low impedance over a wide frequency band as shown in **Fig. 1** .

We have already released Proadlizer products called F-Cases that are employed in videogame machines and notebook PCs but we are still continuing developments aimed at improving characteristics such as lowering the ESR (Equivalent Series Resistance).

With regard to product size, we have added the compact/slim D-Case range (see **Table**) to our lineup in order to meet the design requirements of customers, which include reductions in board sizes and the number of items. The D-Case products have an area that has been reduced by about 26% from that of the F-Case range but still maintain the flat and low impedance characteristics. The external views of D-Case products are

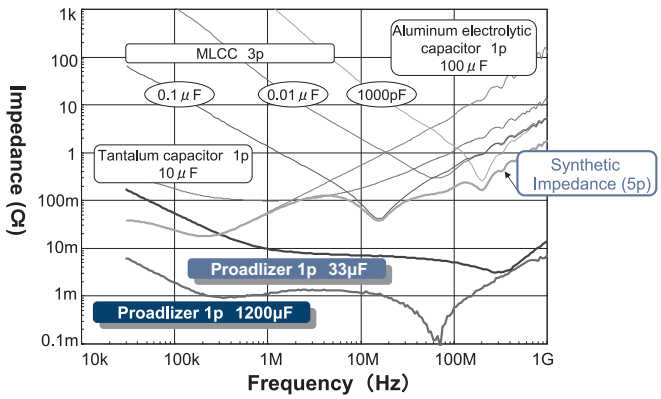

Fig. 1 Frequency characteristics of the Proadlizer impedance.

Table Lineup of the D-Case products.

Model	Dimensions (mm)	Rated Voltage (V)	Capacitance (μF)
PFAD200E336M	9.5× 5.5 × 2.0	2.5	33
PFAD200E107M	9.5× 5.5 × 2.0	2.5	100
PFAD200G226M	9.5× 5.5 × 2.0	4.0	22
PFAD200G476M	9.5× 5.5 × 2.0	4.0	47

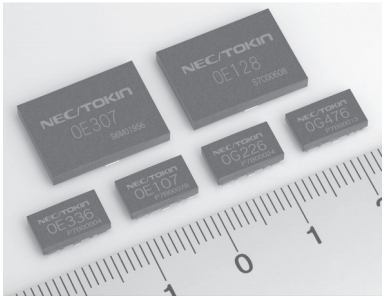

Photo Proadlizer products (Lower row: D-Case products).

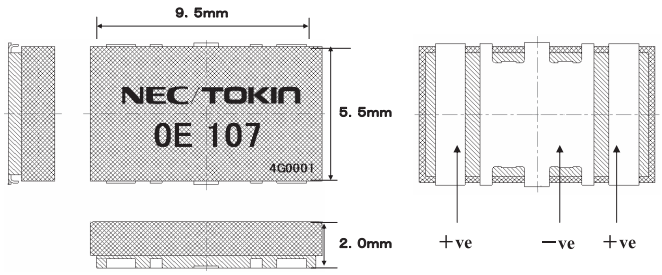

Fig. 2 External view.

shown in the lower row of **Photo** .

3. Features of the Proadlizer

The Proadlizer forms a stripline (transmission line) structure in the internal element in order to achieve flat, low impedance. This structure is usually used in the pattern designs of coaxial cables and high-frequency boards and the Proadlizer is the embodiment of this technology in the form of a capacitor.

Because of this structure, the Proadlizer has two anode terminals one at each end and a cathode terminal at the center as shown in **Fig. 2** . There are two methods used for the Proadlizer design; one is the more usual method called “capacitor design,” in which the anodes at both ends are connected to a single power plane in the inner layer and the cathode is also connected to a single GND plane (**Fig. 3-1**); the other method is the “filtering design,” which is a power supply isolation design connecting the anodes from both sides to a different power plane (**Fig. 3-2**).

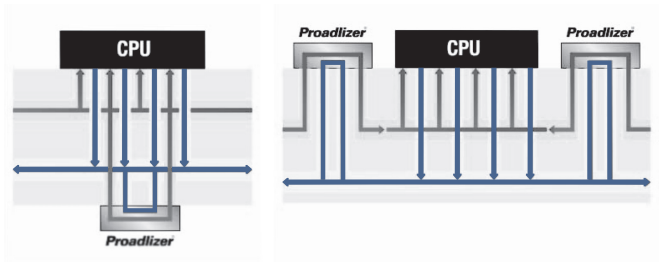

Fig. 3-1 Capacitor design. Fig. 3-2 Filtering design.

Fig. 3 Design methods of Proadlizer.

4. Effect of Power Supply Separation of FPGA–Mounting Boards

The FPGA accepts flexible customization and it was originally used in the prototyping of ASIC (Application Specific Integrated Circuit) or products that are manufactured in small quantities. However, as the performance improved and the cost was reduced, the method began to be used in various network devices, particularly for the base stations of cellular phone, as well as in broadcast equipment and the control circuitry of digital home appliances.

The performance and scale of FPGA are expected to advance in the future but considerations on the reductions of the power voltage and noise are likely to remain, thus making the power supply design a critical matter.

In order to confirm the effect on the Proadlizer of the power supply separation design, we prototyped two kinds of boards by mounting FPGAs, one using traditional capacitors and not using power supply separation and the other using Proadlizer devices and power supply separation. In the case of the board with power supply separation, four slits are formed around the FPGA in the power supply layer in order to separate the FPGA and the power supply and to reduce the emission of FPGA noise to the surroundings by enclosing the noise in the proximity of the FPGA. The board uses four 15μF Proadlizer devices produced in the initial stage of development, places each of them on each slit around the FPGA, and supplies power through the Proadlizer devices. With the board using the traditional capacitors, each set of capacitors was combined using one 10μF device, four 1μF devices and ten 0.1μF devices in order to obtain the same capacitance as each Proadlizer and was placed on each slit. Since the capacitors cannot transmit the power supply, the slits on the board using the traditional 2-terminal capacitors are removed at the positions corresponding to the position of Proadlizer devices on the other board so that the power is supplied from the power supply layer. **Fig. 4** shows the external views and schematic images of the boards mounting FPGAs.

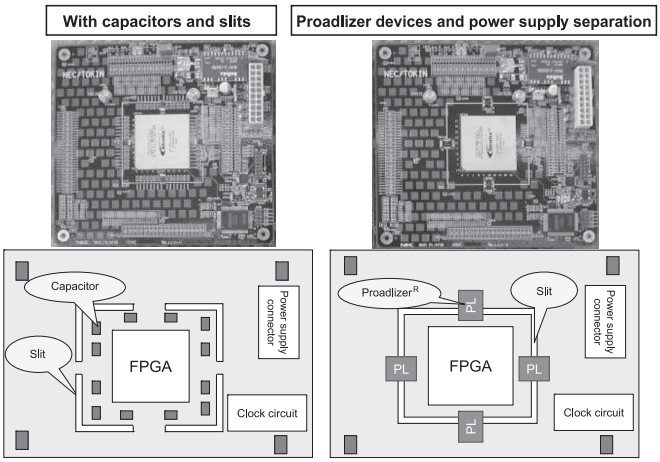

Fig. 4 External views and images of FPGA-mounting boards.

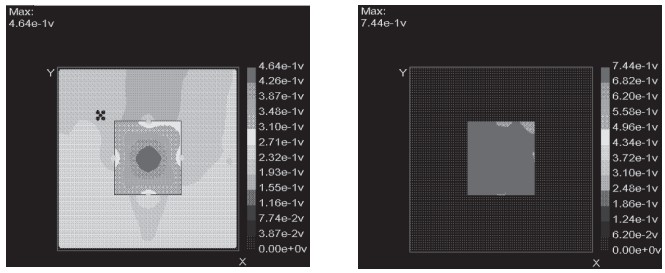

Fig. 5-1
With capacitors and slits

Fig. 5-2
Proadlizer devices and power supply separation

Fig. 5 Results of electrical field distribution simulations.

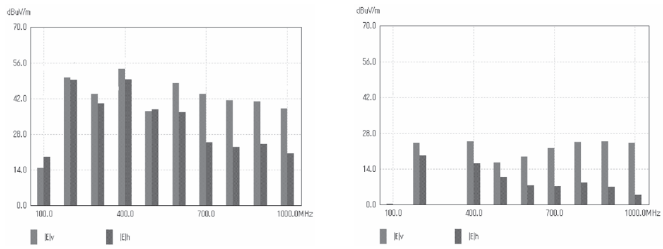

Fig. 6-1
With capacitors and slits

Fig. 6-2
Proadlizer devices and power supply separation

Fig. 6 Results of EMI simulations.

With the prototyped FPGA-mounting boards, we generated a given amount of current fluctuation in the FPGA power supply line and formed multiple registers in the FPGA to evaluate the resulting power voltage variations and EMI. The connections of the registers (Reg) inside the FPGA were inverted, and the output from every other register was led out to the external capacitors. This arrangement makes it possible to output the same power to the external registers and to produce large scale simultaneous operation noise in the FPGA power supply.

Before actual evaluation of the FPGA-mounting boards, we examined their electrical field distributions by conducting magnetic field simulations using their design data. The simulator used was the SPEED2000 of Sigrity, Inc., which is capable of calculating the return voltage and current between the signal and GND and the inter-plane voltage and current between power supply and GND. It may also be applied to decoupling design and EMI analysis of systems.

In order to model the FPGA power supply variation, we connected a 150MHz, 16A triangular wave current source to the FPGA power line position and also connected the SPICE models of the Proadlizer and traditional capacitors respectively to the appropriate positions on the PCB. **Fig. 5** shows the electrical field distributions in the power supply layers of the boards obtained by simulations using the above described arrangements. These results show that high-frequency current is concentrated inside the slits around the FPGA of the board separating the power supply layer with slits. The board using the Proadlizer devices (Fig. 5-2) has a very large high-frequency current enclosing effect resulting from the low impedance of the Proadlizer and the power supply separation with the slits. In the case of the board using the traditional capacitors (Fig. 5-1), the effect of the slits is not obtained fully because the slits are not continuous; a part of the high-frequency current leaks from the spaces in the slits so that the voltage fluctuation is spread all over the board.

Fig. 6 shows the results of simulations of the radiation noise emitted from the boards. In general, the radiation noise from a board increases when high-frequency current is widely distributed on the board. The results of the simulations also reflected the field distribution results above, and the board using the Proadlizer devices and slits that presented the lower voltage fluctuation (Fig. 6-2) emitted lower radiation noise.

Then, we actually ran the boards and measured the noise superimposed in the power supply lines. We connected a probe on the measurement terminals 1 and 2 on each board and measured the noise superimposed on the voltage using an oscilloscope. Terminal 1 was installed at a point that could obtain the core voltage near to the center of the FPGA through the inner layer, and Terminal 2 was installed at a point near the output of the on-board power supply. **Fig. 7** shows the positions of the measuring points and **Fig. 8** shows the results of

power noise measurements. In each noise waveform measurement result, the upper waveform is the clock waveform, the middle one is the noise waveform measured at Terminal 1 and the lower one is that measured at Terminal 2. What is common to both boards is that the power line noise is generated synchronously with the rise of the clock and that the noise immediately below the FPGA, measured at Terminal 1, is larger than the point near to the on-board power supply output measured at Terminal 2. In comparative terms, the boards featuring the power supply separation design and Proadlizer devices emitted lower noise and better results than the other boards.

Next, we measured the magnetic fields in close proximity.

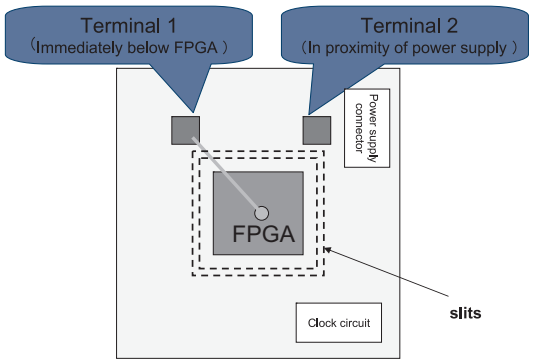

Fig. 7 Voltage measuring points on the power supply layer.

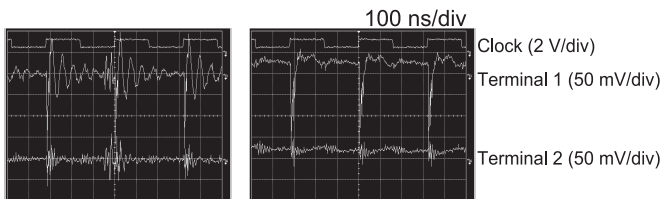

Fig. 8-1
With capacitors and slits

Fig. 8-2
Proadlizer devices and power supply separation

Fig. 8 Results of noise measurements.

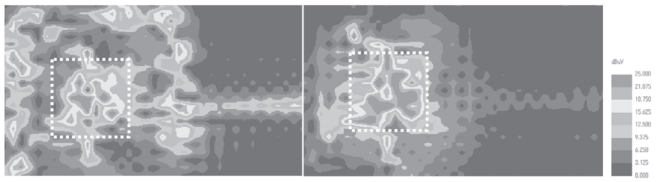

Fig. 9-1
With capacitors and slits

Fig. 9-2
Proadlizer devices and power supply separation

Fig. 9 Results of nearby magnetic field measurements.

We installed and drove each FPGA-mounting board on the table of a PCB magnetic wave measurement system, scanned the board surface by dividing it into fine-mesh areas, and measured the noise level of each area.

For a board with traditional capacitors, noise was observed over the whole of the board and for a board using a power supply separation design and Proadlizer devices, noise was present only inside the power-separating slits and was hardly found at all outside them.

The results of the nearby magnetic field measurements (**Fig. 9**) very much resemble those of the electrical field distribution simulations (Fig. 5). In this way, we were able to demonstrate the overall tendency by means of advance simulations as well as by various evaluations and demonstrations using actual products.

5. Effectiveness of Power Supply Separation

In section 4 above, we discussed the effects of using power supply separation and Proadlizer devices. The main markets in which this design method is expected to be effective may include the networking market including the main board of cellular stations and communication equipment as well as for the markets handling sets that feature space saving and multiple functions.

If the traditional design concept was used to deal with markets in which the anti-noise and EMI (Electromagnetic Interference) designs are critical, it would be necessary to overcome various issues such as providing countermeasures against the resonance resulting from the use of multiple laminated ceramic capacitors, the consequent increase in the number of components following utilization of the above countermeasures and the increase in the space requirement. We believe that the use of Proadlizer devices and power supply separation under such circumstances is advantageous when compared with the traditional design because the system makes it possible to apply requisite measures at the design stage.

6. Conclusion

The recent technological trends in chip design such as diversification and increased speeds have tended to require enhanced peripheral devices. The Proadlizer is capable of dealing with such trends by providing advantages from various aspects. These include low impedance over a wide frequency

band as well as the noise suppression function provided by the power supply separation design. In the future, we intend to expand the product series and further decrease costs in order to provide more attractive benefits for our customers.

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