

“NaviEngine 1,” System LSI for SMP-Based Car Navigation Systems

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Abstract

NEC Electronics has succeeded in developing NaviEngine 1, a system LSI for car navigation systems, thus achieving a world first use of the SMP type multicore. This paper is intended to introduce recent trends in the car navigation market. It also discusses the multicore technology used as the basis of development as well as the versatile features of NaviEngine 1 including the graphics and LCD controller functions.

In addition, this paper also discusses details of the development of the NaviEngine 1. These include techniques for achieving the high quality required for devices in car-mount equipment, the pre-evaluation of software to ensure high performance of the multicore LSI and the procedures adopted for creating an optimum development environment.

Keywords

car navigation, multicore, SMP, graphics, LCD controller, serial ATA, car-mount capability
high quality, software development environment

1. Introduction

1.1 Car Navigation Market Trends

In Japan, it is not unusual to see car navigation systems mounted in the taxis that pick up people on the streets and in the vehicles used by the general population. Also, in many overseas countries, we often see PNDs (Portable Navigation Devices) sold as an everyday commodity at airport shops, etc. At present, car navigation systems are being sold in the world car navigation market at the rate of more than 10 million units per year and as shown in **Fig. 1**, they are expected to contribute to a future improvement in vehicle safety by utilizing car-mounted cameras.

At NEC Electronics, we regard the car navigation field as a market to be closely monitored, as we predict that it will evolve into the core technology for the implementation of intelligent vehicles. In this context we have been making efforts to establish semiconductor chip solutions that are focused on the microcomputer.

1.2 Multicore Technology

When we review the technical trends in the field of microcomputers, we see that the multicore technology has recently

been developing rapidly and increasing in importance. The SoC (System on Chip) technology based on multicore technology is being used widely for video game machines, cellular phone handsets and digital home appliances.

In particular, it is used in the fields that have the highest performance requirements such as for car navigation systems. In general, attention is shifting from the traditional asymmetrical multicore technology that implements a function-distributed system in which the functions are allocated inflexibly to specialized microcomputers and DSP devices. This system is being replaced by a symmetrical multicore technology that

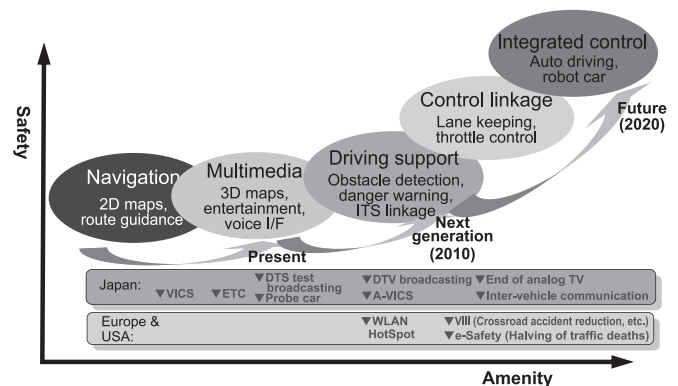


Fig. 1 Predictions for car navigation systems toward 2020.

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implements a load-distribution system in which functions are allocated dynamically as required.

At NEC Electronics, over the last two decades we have been conducting research in collaboration with NEC Central Research Laboratories into the development of multicore technologies, as shown in Fig. 2 .

As a result, we were able to announce the MP98 technology in 2000 and released the MP211 range as the SoCs for the cellular phone field in 2005.

Recently, we have succeeded in developing the NaviEngine 1, an SoC product for car navigation systems that adopts the SMP (Symmetrical Multicore Processor) technology for the first time in the field. This product can be used to build a multifunction high-performance car navigation system as shown in Fig. 3 .

In the following sections, we will introduce the features of

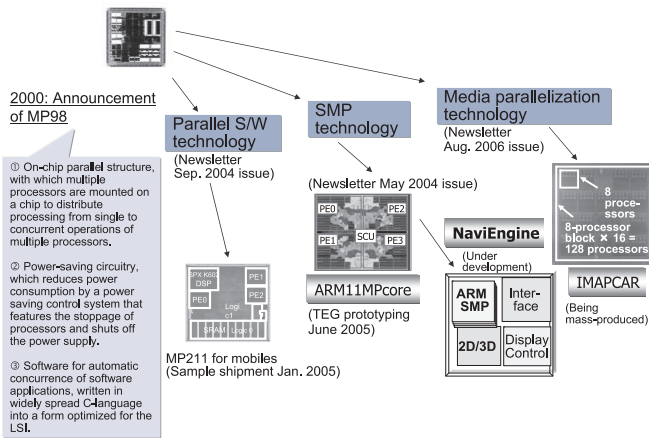


Fig. 2 Multicore products from NEC.

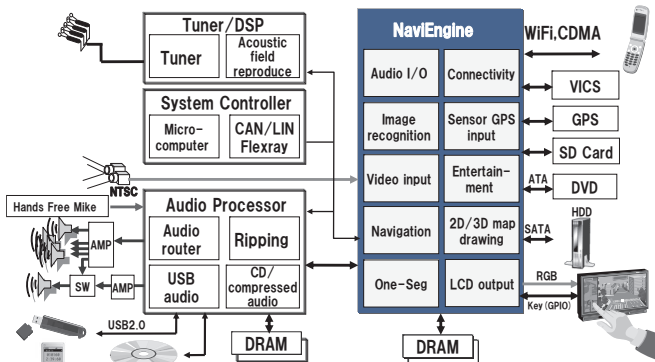


Fig. 3 NaviEngine-based car navigation system.

the NaviEngine 1 device, features of the development of the SoC product and the software development environment required for the multicore technology.

2. Features of NaviEngine

2.1 MPCore

The NaviEngine 1 uses the MPCore multiprocessors of ARM as the CPU core. MPCore is a RISC multiprocessor compatible with the ARMv6 and Thumb instruction sets as well as the SIMD instructions and Jazzele (high-speed Java processing technology).

The main features of the MPCore are as follows:

- CPU cores: ARM11 microprocessor architecture CPU x4.
- Built-in large-capacity primary cache memory.
- Instruction caches: 32K bytes per CPU.
- Data caches: 32K bytes per CPU.
- 8-stage pipeline architecture with branching prediction and hold functions.
- One VFP coprocessor in each CPU.
- Maximum operation frequency: 400 MHz.
- Processing performance: 1920 DMIPS.
- System buses: Dual 64-bit AMBA3 AXI system buses.
- Cache coherency: Optimized MESI coherency protocol for improved processing efficiency.

The use of a high-performance MPCore optimizes NaviEngine 1 for multifunction, high-performance car navigation systems with high processing capabilities including multimedia processing and drive support based on image recognition.

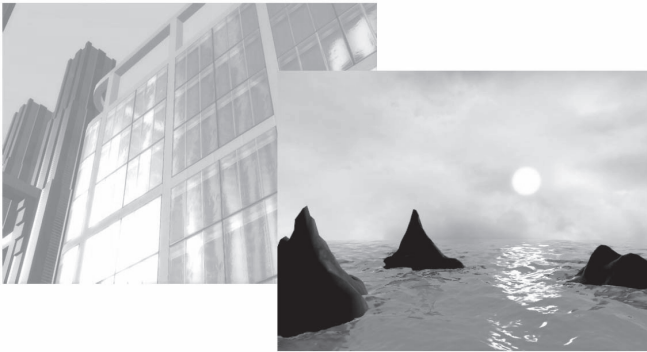
2.2 2D/3D Graphics Engine

For the 2D/3D graphics engine, which is indispensable for car navigation systems, the NaviEngine 1 uses the SGX535, which is a high-performance GPU (Graphics Processor Unit) compatible with new-generation architectures that belongs to the PowerVR SGX family of Imagination Technologies.

The SGX535 adopting programmable shaders of the new-generation architecture, draws high-definition 3D images as shown in Fig. 4 and achieves simultaneous 2D and 3D image drawing using the multithread configuration. Fig. 5 shows the block diagram of the SGX535.

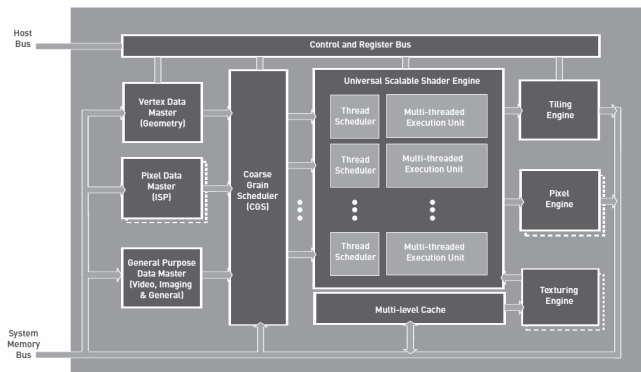
The main features of the SGX535 are as follows.

- Two universal scalable shader engines (USSEs) are built



Images supplied by Imagination Technologies.

Fig. 4 Image drawing by PowerVR SGX.



Images supplied by Imagination Technologies.

Fig. 5 Block diagram of PowerVR SGX.

in to enable programmable vertex and pixel processing.

- Tiling system for reduced memory band load.
- All of the 3D functions of OpenGL 2.0, OpenGL ES2.0 and DirectX9 built in.
- Multi-thread capability for simultaneous 2D/3D image drawing.
- Image drawing core performance at the highest level in the industry.
- Vertex processing performance: 15M polygons/sec.
- Pixel drawing performance: Approx. 800M pixels/sec. (considering the hidden image erasure effect).

2.3 Display controller

The NaviEngine 1 incorporates a display controller optimized for the AVN (Audio Visual Navigation) car navigation systems with a multimedia processing compatibility.

The main features of the display controller are as follows.

- 7-layer screen synthesis with multi-window and high-definition map drawing capabilities.
- WSVGA (1024 × 600 pixels) high-definition display capability: Compatible with up to WXGA (1280 × 768 pixels) by limiting the number of layers.
- Versatile transmission functions (layer transmission, pixel transmission, color key (chroma keying)).
- Independent magnification/reduction capabilities for each layer.
- Image correction functions (dizzer, brightness, gamma correction)
- Hardware cursor built in.
- Roundlap capability.

2.4 Other IPs

The NaviEngine additionally incorporates a middleware-based One-Seg playing capability, a TS (Transport Stream) interface enabling image recognition and a video capture function in order to benefit from the high processing capabilities of MPCore. In consideration of the shifting of the PC HDD market from the ATA interface to the serial ATA interface the ATA and serial ATA interfaces are also incorporated. In addition, it is also equipped with AVN features such as two ports for USB hosts, which takes into account the need for connectivity with cellular phone terminals.

3. Points in SoC Development

3.1 Features of Internal Architecture

Fig. 6 shows the internal block diagram of the NaviEngine 1. We developed NaviEngine 1 with reduced TAT in accordance with our corporate policy of developing car navigation SoC products as platforms. Particularly, with regard to the display, video capture and 2D/3D graphics functions that need high bus performances, we improved the throughputs by adopting the AXIS bus, which is a multilayer bus, following the output ports of MPCore. We also gave MPCore a 4-CPU configuration by placing importance on the processing performance.

3.2 Measures Considering Car-Mount Applications

Since the characteristics of car-mount products necessitate a defective ratio of less than 10ppm, we set the target fault

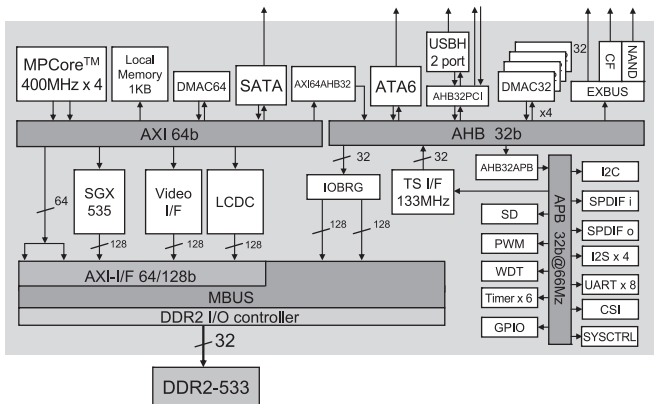
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Fig. 6 Block diagram of NaviEngine 1.

detection rates at more than 99% for individual stuck-at faults and more than 97.5% for transition faults. In order to achieve these results, we employed the DFT (Design for Testing) technique totally and adopted the logic BIST and memory BIST of Logic Vision, Inc. with NaviEngine 1. We also incorporated individual test modes for the mounted hardware and macro functions and, for the clock divider circuit, faults that cannot be detected with the logic BIST due to its principle configuration, provided a function for monitoring the clock from outside. These measures have made it possible to attain the target fault detection rates.

3.3 Improvements in Development Efficiency

In order to mount the logic BIST and memory BIST in a short period, we conducted development in collaboration with the Technology Centre of NEC Electronics Europe, which was a pioneer in this field. During this process, the time difference between Japan and Europe served to conduct data generation and verification work very efficiently.

As NaviEngine 1 incorporates more than five macros that were completely new designs, the risk of intervention of design troubles was larger than for other products. To deal with this contingency, the development team set a slogan of “perfect ES operation from the first trial,” fabricated a prototype using FPGA and evaluated it whenever possible in an actual operational environment. As a result, for the ES of NaviEngine 1, we succeeded in meeting the aims of our slogan without major bugs.

4. Software Development Environment

4.1 Issues in Software for Multicore Systems

The NaviEngine 1 adopted the SMP multicore technology as a revolutionary application for car navigation systems. This has posed the following major issues with regard to software development; 1) The need to confirm the effectiveness of a multicore solution for the target system; 2) to run the huge amount of existing software (including that for single-core systems and that tuned for embedding) on the multicore OS; 3) to redesign the software structure as one with excellent extension and diverted use capabilities, in order to use the hardware at its maximum performance capability. It will be after solving these issues that a high-performance system capable of utilizing the full performance of NaviEngine 1 in a short period will be realized. However, these issues will not actually be easy to solve quickly, considering the amount of existing software and the complexity of the software for multicore systems.

Therefore, we decided to adopt a realistic course of action in order to advance multicore capability by solving the issues step by step in the order from 1) to 2) and 3) and so on.

4.2 Measures Taken with NaviEngine 1

To solve issue 1) above, we first created in 2005 to 2006 when NaviEngine 1 and the SMPOS did not yet exist, an original tool to implement the analysis of parallel application operations. Using this tool, we confirmed that the system performance can be improved even when existing car navigation software is run on NaviEngine 1 with small enough overhead (performance degradation) as an SMP operation mechanism and that the NaviEngine 1 is useful with car navigation software. This result and other results of analysis were fed back to the SoC design in order to improve its effectiveness.

4.3 OS Compatibility, etc.

What is important for the provision of multicore compatibility for software are the embedded software development tools such as the debugger, system analysis tool and tuning tool. Several kinds of multicore compatible ICEs (In-Circuit Emulators) that can be connected to NaviEngine 1 are already available. Other software tools including the OS are being developed by tool vendors and forums and will be available one after the other. As expansion of these tools is expected to pre-

pare the environments for solving issues 2) and 3), we are positively promoting activities that comprise collaboration with third parties.

5. Future Deployment

At NEC Electronics, we do not position the NaviEngine as an individual product but regard it as a basic architecture centered around the following technologies:

- Scalability of multicore systems.
- High-performance internal buses reserving the necessary bandwidths.
- Graphics engine providing a high-quality user interface.

In the future, we plan to develop several SoC chips based on this architecture and to deploy them in new products. We believe that this will allow the users of the NaviEngine to develop over several generations to come, a large number of car navigation products aimed at different customer groups.

We will also improve basic architectures in order to continuously improve performance, reduce power consumption and enhance cost efficiency and make proposals for increasing the added values of car navigation products by means of middle-ware, etc.

6. Conclusion

The newly developed NaviEngine 1 is an SoC product designed to become the core of the car navigation systems that are expected to increase in importance in the future. We will also advance the architecture of the NaviEngine in order to effectively make it the brain of vehicle systems.

Recent developments have allowed us to establish the flow for the development of large-scale integrated SoCs of a high enough quality for car-mount use, by adopting the most advanced processes that have been designed to offer high performance and advanced functions. This expertise will not be limited in its range of applications to car-mounted equipment but will also serve as important assets for us in the development of large-scale SoC products in the future.

We are currently building a multicore software development platform based on the NaviEngine. This platform will accommodate multicore-compatible software based on our multicore technology as well as on the technologies of third parties. It is expected that it will provide users with a wide range of functional options.

By means of these activities, we hope to further improve our competence in the development of microcomputers and SoC products.

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