A New High-k Transistor Technology Implemented in Accordance with the 55nm Design Rule Process

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Abstract

NEC Electronics has developed a transistor that delivers low current leakage, high performance and a significant reduction in the manufacturing processes. These solutions have been achieved by establishing a threshold voltage control technology to control the work function by applying a trace of hafnium to the gate insulation film of a transistor. This paper introduces the 55nm (nanometer) node design rule CMOS process technology, "UX7LS" which combines the above new transistor technology and the immersion lithography technology. UX7LS enables a wide variety of applications to be covered with a single transistor structure by controlling the threshold voltage, between 0.3V to 0.5V. Moreover, a performance increase of approximately 20%, a process decrease of maximum 15% and scaling down of the SRAM cell size to 0.446μm² have been achieved compared to the performance of transistors that conform to the 65nm design rule.

Keywords

High-k gate insulation film, hafnium silicate, work function control, 55nm node CMOS, ArF immersion lithography, manufacturing process reduction

1. Introduction

The scaling down of the transistor threshold voltage (Vth) and gate oxide film thickness has been accelerating in recent years and this has resulted in increases in the standby power consumption, which has become a severe problem, especially in the mobile phone LSI market. As a result of reducing the gate insulation film thickness, the gate leakage current increases tenfold by a reduction of 0.2nm. In order to reduce the gate leakage current, the introduction of High-k (high-dielectric constant) gate insulator film which is a new type of insulation film as a replacement for the conventional silicone oxide film has been promoted since 2000. In 2004, NEC Electronics and NEC Corporation co-developed a low leakage current transistor[1] employing hafnium silicate (HfSiO) and tested it for LSI chip suitability for mobile phone use[2]. This low leakage current transistor features 1/1000th or less of current leakage compared to that of conventional silicone oxynitridation film, and negligible carrier mobility degradation. However, it is difficult to fabricate the low Vth (threshold voltage) transistors with this technology. Therefore, available applications are limited to the LSIs designed for high Vth transistors.

NEC Electronics has focused on the new employment of hafnium[3] to establish a transistor technology with a low leakage current, high performance and a significant reduction in the manufacturing processes. By combining this technology with the immersion lithography, the 55nm (nanometer) node design rule CMOS process technology, "UX7LS" has been developed. UX7LS enables coverage of a wide variety of applications, by controlling the Vth between 0.3 to 0.5V (OFF leakage current: 30pA to 3nA) (**Fig. 1**). Moreover, performance increases of approximately 20%, process decrease of max. 15% and the scaling down of the SRAM cell size to 0.446μm² have been achieved (0.525μm² with 65nm node design rule).

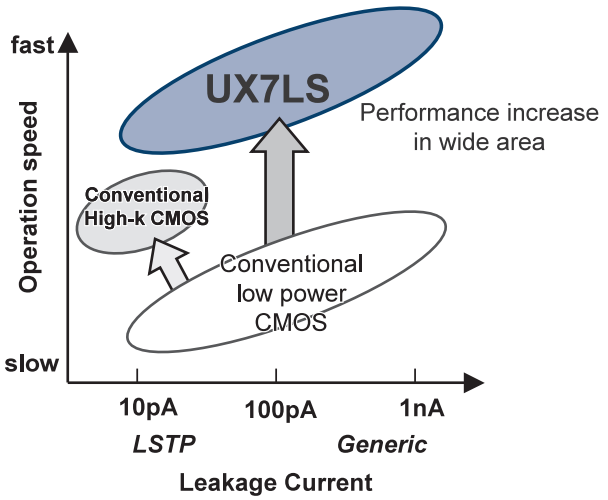

Fig. 1 UX7LS process performance increase concept.

2. High Performance Transistors with Hafnium Silicate

With the conventional transistors with Vth of 0.3V to 0.5V which are generally used for mobile phones and general purpose devices, the Vth are adjusted by large amount of channel impurity. However, when channel impurity increases, electron and hole carriers disperse during passing through the channel and the carrier mobility decreases. Also, the more impurities concentrated in the channel, the larger the junction leakage current between the source / drain and the substrate becomes.

To solve this problem, another method has been developed to control the Vth by attaching hafnium on the gate insulation film instead of concentrating more channel impurity. **Fig. 2** shows the variation of the Vth and the amount of hafnium contained in the gate insulation film. It used to be difficult to control the Vth with a conventional High-k gate insulation film because the fermi level pinning effect occurred and the Vth was significantly increased. If the amount of hafnium is decreased, the Vth can be suppressed by 0.1V to 0.2V. This phenomenon indicates that transistor performance can be increased without thinning the gate insulation film if the Vth can be controlled by the addition of a small amount of hafnium (work function control).

Fig. 3 shows the comparison of the transconductance between cases in which the conventional method, which is the Vth is controlled by channel impurities, and the new method, in which the work function is controlled by applying hafnium. When adopting the method of the Vth is controlled by concentrating channel impurities, the transconductance (gm) decreases according to the increase in the Vth or channel impurities. However, when the method of the work function control by applying hafnium, the gm does not decrease even when the Vth increases. The UX7LS process enables the formation of transistors with Vth of 0.3V to 0.5V on single chips by employing both methods to control the Vth by applying hafnium and by concentrating channel impurities with the best balance.

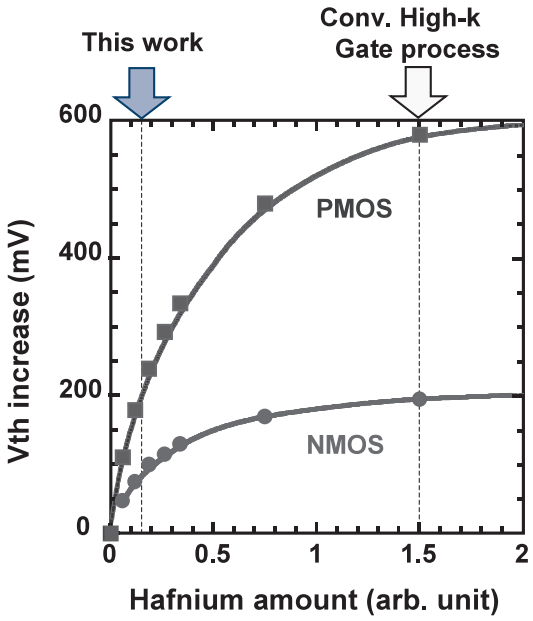

Fig. 2 Hafnium amount and threshold voltage contained in a gate insulation film.

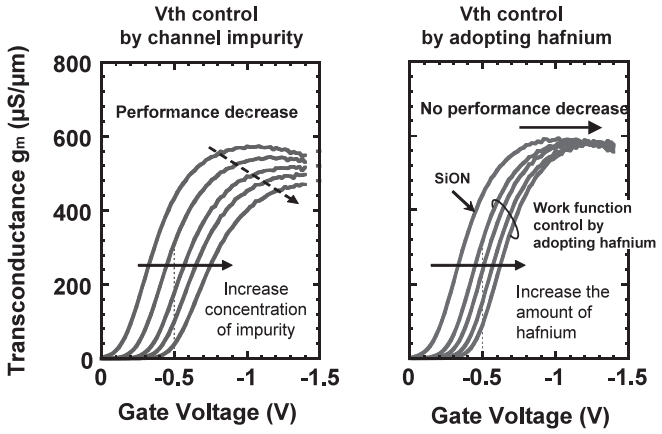

Fig. 3 Transistor performance increase with work function control.

3. 55nm Node CMOS "UX7LS" Process

The 55nm node CMOS "UX7LS" process has been developed by employing the work function control technology using hafnium.

Fig. 4 shows a photograph of a transmission electron microscope (TEM) cross section of a transistor manufactured by the UX7LS process. The photo on the right of Fig. 4 is an enlarged one of a gate insulation film. With the conventional High-k insulation film, the film thickness proportion of HfSiO film and SiON film are 1:1. With the UX7LS process, the amount of the hafnium can be decreased to very little, so that the film thickness proportion of HfSiO film and SiON film can be arranged with 1:5. or less. This enables superior control of the Vth by the work function control.

Fig. 5 shows comparison of the ON/OFF current relationship with the UX7LS processing transistor and 65nm node transistors of other manufacturer's. The UX7LS processing transistor

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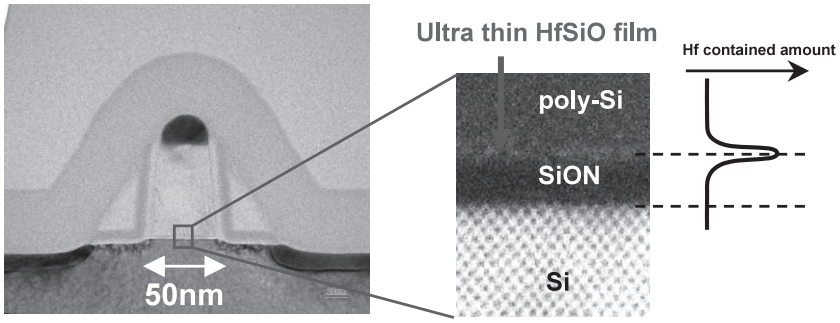

Fig. 4 Cross sectional TEM image of a transistor.

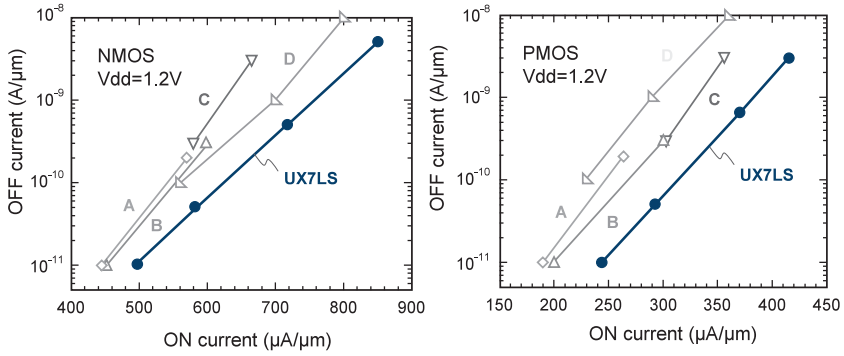

Fig. 5 Transistor performance comparison.

has achieved an ON current of 575/290μA/μm (OFF current of 55pA/μm) with a power supply voltage (Vdd) of 1.2V. This shows a better performance by approx. 20% than those of other manufacturer's 65nm node transistors. The UX7LS also demonstrates a superior performance when used in low standby power consumption devices and in low operation power devices.

Channel impurity concentrations of transistors can be reduced with the UX7LS process, so that GIDL (Gate Induced Drain Leakage) and junction leakage current are also expected to be decreased. **Fig. 6** shows the GIDL and junction leakage current of PMOSs, one manufactured by the UX7LS process and the other manufactured by the conventional SiON film.

The result shows that the leakage current is decreased especially in the high Vth by employing a work function control technology. This indicates that the UX7LS processing transistor is most suitable for SRAM and DRAM, which require a low leakage current design.

When HfSiO film is employed as a gate insulation film, there is concern regarding its performance reliability. **Fig. 7** shows the TDDB (Time Dependent Dielectric Breakdown) characteristics of NMOS and PMOS at 110°C. When a power law model is employed, the estimated time to break down of a gate insulation film is over ten years for 1.3V. By optimizing the HfSiO film forming process, the UX7LS process has thus assured an adequate time to break down for a gate oxide film mounted on a practical product.

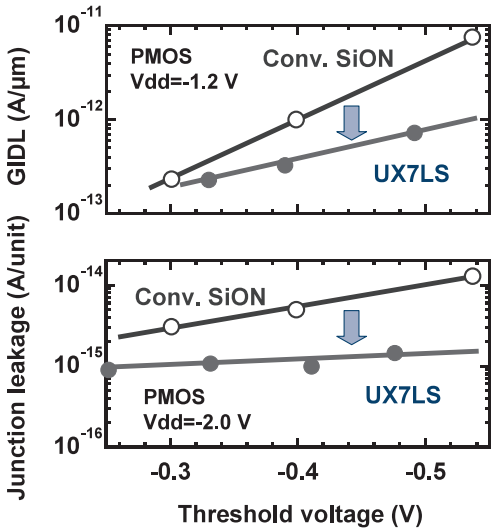

Fig. 6 Vth dependency on GILD and junction leakage current.

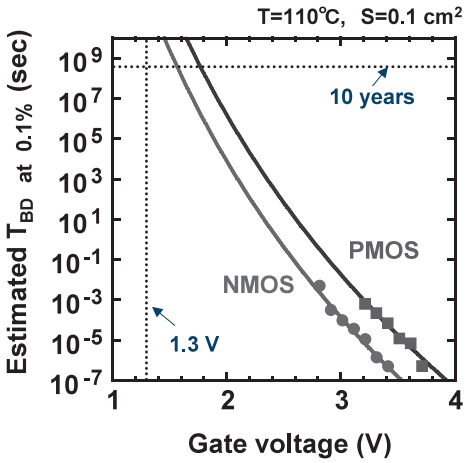

Fig. 7 Gate insulation film reliability.

Work function control using hafnium provides significant effectiveness in reducing steps of manufacturing process as well as in increasing the transistor performance of a transistor. **Fig. 8** is a comparison of Vth for various channel widths between a conventionally manufactured 90nm node transistor and a UX7LS processed transistor. The Y axis shows the differentiation of the Vth from the Vth at a channel width of 1.0μm. As is shown in the graph of Fig. 8, with a conventional transistor the Vth decreases in the graph area where the channel widths are narrow. This phenomenon is called the "inverse narrow channel effect". With a UX7LS processing transistor, this phenomenon does not appear. The "Inverse narrow channel effect" is considered as a phenomenon occurring due to channel impurities being dispersed at the boundary of the element isolation oxide film. With the UX7LS process, this "inverse narrow channel effect" hardly occurs because the Vth is controlled by the work function control technology.

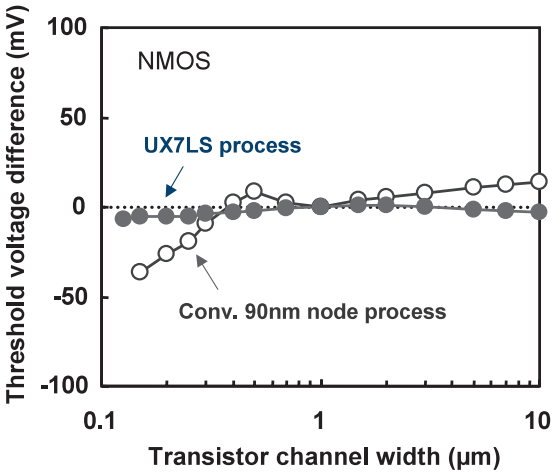

Fig. 8 Vth dependency on the transistor channel width.

In order to prevent the "inverse narrow channel effect" with the conventional technology, additional ion implantation process are required for SRAM cell transistors with minimum channel width used. On the other hand, with a UX7LS processing transistor, the "inverse narrow channel effect" hardly occurs so that the ion implantation process to the SRAM cell transistors and the logic section transistors can be carried out as the same process. This solution has resulted in a significant decrease in the manufacturing processes.

Common processing of ion implantation for other transistors has also been examined, and decreasing the processing of five masks at maximum, which is equivalent to an approximate15% decrease in the manufacturing process (in comparison with the process of a 65nm node FEOL manufactured by NEC Electronics), has been achieved with the UX7LS process.

Fig. 9 shows SEM (Scanning Electron Microscope) image of an SRAM cell (cell size: 0.446μm²) after the gate polysilicon etching. The UX7LS process has employed immersion lithography technology for the first time in the world market. By employing an ArF immersion lithography with a high NA (Numerical Aperture), the formation of fine patterns with minor size fluctuations has become possible, thus enabling development of the worlds smallest SRAM.

To conclude this paper, the design rule of the UX7LS process is explained in **Table**. With the UX7LS process, a variety of downsizing has been achieved including equivalent oxide

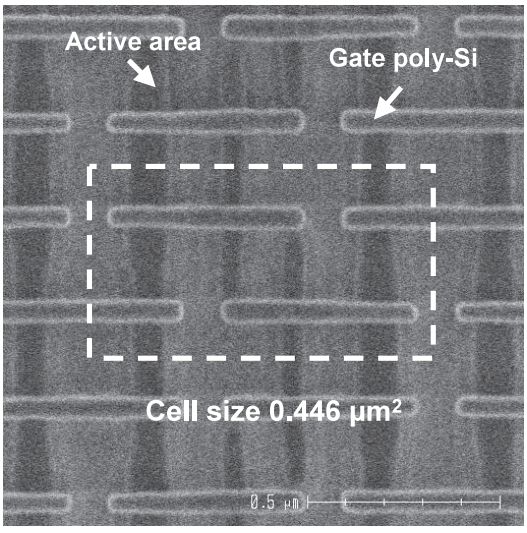

Fig. 9 SEM image of SRAM cell (top view).

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Table UX7LS process design rule.

Logic node (nm)	55
Supply Voltage (V)	1.2
EOT (nm)	1.85
Gate L/S (nm)	50/130
Contact L/S (nm)	80/100
Metal 1 L/S (nm)	80/80
Metal 2 L/S (nm)	90/90
SRAM Cell Size (μm^2)	0.446

thickness (EOT) of the gate insulation film thickness to 1.85nm, gate electrode length to 50nm and first metal pitch to 160nm. Such downsizing has resulted in an integration percentage of more than twice those of the 90nm node design rule, which is widely adopted in the market.

4. Conclusion

NEC Electronics has developed a 55nm node CMOS process technology "UX7LS" which enables low standby power consumption and high-speed operation. By developing a High-k technology different from the conventional technology, a variable Vth and high performance have been achieved so that a single transistor structure may be employed for various devices. These include the mobile phone which requires an ultra low standby power consumption to high-speed logic devices that require a high drive current. Moreover, miniaturization of the SRAM cell size to 0.446μm^2 has been achieved by employing immersion lithography technology.

With the UX7LS process technology, NEC Electronics is able to market system LSIs that feature low power consumption and high-speed performance for a wide variety of applications fields, including the mobile phone and networking markets.

References

1) Y. Yasuda et al., 2004 Symp. on VLSI Tech., 40.
2) N. Kimizuka et al., 2005 Symp. on VLSI Tech., 218.
3) H. Nakamura et al., 2006 Symp. on VLSI Tech.,198

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