“EMMA2RH,” an LSI Chip for DVD Recorders That Enables the Simultaneous Recording of Two HDTV Programs

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Abstract

NEC Electronics has developed a single-chip LSI that enables simultaneous receiving and recording of two digital Hi-Vision (HDTV) programs. This LSI integrates two functions onto a single ship. These are the HDTV function that includes terrestrial digital broadcast receiving and the DVD recorder function. These functions are used by being mounted onto two different function units. This LSI technology is a world first and with it high performance and low cost have both been achieved at the same time as providing the most appropriate solutions for users.

Keywords

HDTV broadcasting, DVD recorder, system LSI, stream processor, MPEG, Linux, RTOS

1. Introduction

In recent years, areas that can receive BS digital broadcasting and terrestrial digital HDTV broadcasting have expanded. This situation has correspondingly resulted in the rapid development of TV sets for digital Hi-Vision programs. Accordingly, the demands of users have been increasing so that they may benefit from the reception of better quality pictures. This trend is expected to support the spread of Hi-Vision recorders in the near future that are capable of recording HDTV programs without any degradation of the picture quality. The price of HDTV set-top boxes is shifting to suit the broader market so that the development of a system LSI that enables both high performance and a decrease in the system cost is strongly desirable.

In consideration of such a market trend NEC Electronics has marketed “EMMA2RH,” a system LSI chip that integrates an HDTV LSI chip and a DVD recorder LSI chip that are capable of HDTV programs.

2. Features of EMMA2RH

The features of EMMA2RH are;

(1) DVD Recorder Optimization Capable of HDTV Broadcasting

The capability of simultaneous recorder operation that is suitable for digital Hi-Vision Recorder, such as the simultaneous receiving and recording of two HDTV programs with a single LSI chip.

(2) High Performance Stream Processor

The provision of a flexible high-speed stream processing function that can be adapted to operate with a next-generation DVD recorder (HD DVD and Blu-ray).

(3) Architecture Employing Two CPUs

EMMA2RH incorporates a main CPU and a sub CPU that are used separately for applications and drivers. Real-time processing is processed at the sub CPU so that the main CPU is open for user applications. The architecture dividing functions between these two CPUs provides an environment for DVD manufacturers to mount functions that can differentiate their products from those of other manufacturers.

A block diagram of EMMA2RH is shown in **Fig. 1**, and its specifications are shown in **Table**.

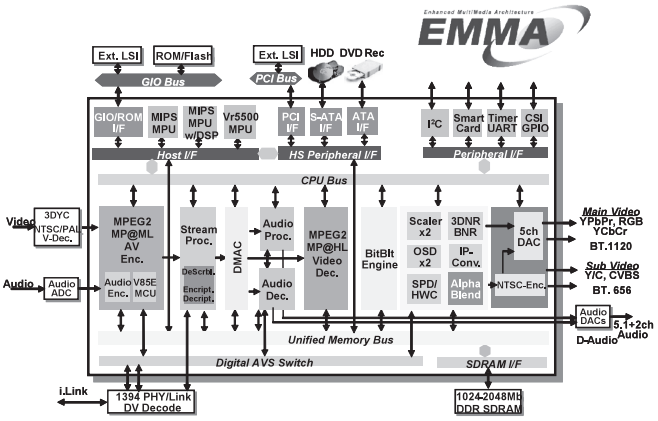

Fig. 1 EMMA2RH block diagram.

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Table Specifications of EMMA2RH.

Item	Specifications
Video	NTSC Video Encoder Component output/5 ch video DAC for S video output ITU-R BT.656 input: 2 ITU-R BT.1120/1358/656 output: 1, ITU-R BT. 656 output: 1
Audio	PCM audio input: 2, 5.1ch+Down Mix PCM audio output:1
Encode	MPEG2 video MP@ML standard, MPEG1 standard
	MPEG1 audio layer 2 standard, LPCM for DVD Dolby Digital consumer encode (family option)
Decode	MPEG2 video MP@HL,MP@ML standard, MPEG1 video standard
	Main audio Dolby Digital, MPEG1 audio layer 1/2, LPCM for DVD, family option: MP3, WMA, MPEG2 AAC-LC
	Sub audio Dolby Digital, MPEG1 audio layer 1/2, LPCM for DVD, family option: MPEG2 AAC-LC
Memory interface	DDR333 64-bit bus width DDR SDRAM
ATA interface	Ultra-ATA100 bus master mode compatible parallel ATA / ATAPI 1.5Gbps serial ATA interface: 3
MPEG system	MPEG2-TS, DVD-Video, DVD-Video recording, DVD+VR, Video CD 2.0
Peripherals	UART, clocked serial interface , SmartCard interfaces, I2C, IR transmitter interface
Power supply/Voltage	3.3V I/O, 2.5V (DDR SDRAM interface), 1.5V (core logic), 1.57V (S-ATA)
Package	641-pin Plastic BGA (35mm by 35mm)

3. Outline of EMMA2RH Functions

3.1 CPU

NEC Electronics original 64-bit MIPS CPU VR5500 is employed for the main CPU. This is a high performance and flexible CPU that incorporates a 32Kbyte instruction cash memory and data cash memory that are capable of various applications.

The sub CPU employs a 32-bit MISP32 CPU of the MIPS Technology Inc. It incorporates an 8Kbyte instruction cash memory and a data cash memory to control the AV processing for which a real-time processing capability is required.

3.2 Stream Processor

This is NEC Electronics' original processor designed exclusively for stream processing. It is flexibly capable of the next-generation DVD standards as well as various streaming signals such as DVD Video, DVD Video recording, DVD +VR and Video CD.

3.3 MPEG Video Decode Engine

An MPEG video decoder engine complying with MPEG2 MP@HL and MPEG1 formats is incorporated. EMMA2RH is capable of a dual decode of MPEG2 MP@HL + MPEG 2MP@HL (SD quality down convert) so that it enables re-encoding and recording a program with DVD-Video recording format while watching another HDTV program. Moreover, the entire operation may be processed with a 2Gbit memory thanks to NEC's original bandwidth compression decode architecture.

3.4 Audio Decode Engine

A dual audio decode engine is mounted. A 32-bit MIPS32 CPU is employed as the main decoder so that various audio formats and virtual sound are available.

The sub decoder is composed of NEC Electronics' original processor, which is used exclusively for audio signals so that it is capable of various formats in a similar way to the main decoder.

3.5 The MPEG Encode and Audio Encode Engine

Based on the proven MPEG2 encoder of NEC Electronics LSI, these are integrated as core functions on a single chip especially for EMMA2RH. The video encoder is capable of the MPEG2 MP@ML and MPEG1 formats and the audio encoder is capable of MPEG1 layer 2 and Dolby Digital consumer encoder formats.

3.6 Unified Memory Architecture

Unified memory architecture can process the data transmission commands of all of the units that use the memory, by using a single interface/SDRAM and this architecture may thus significantly reduce the system cost. A DDR SDRAM interface with 166MHz and 64-bit width is mounted, which features up to 2,048Mbit DDR SDRAM.

3.7 DMA Controller

This controller can process subsequent DMA transmissions without using a CPU: 1) between an internal unit (TS input/demultiplexer, MPEG decoder engine or an audio decoder engine) and an SDRAM, 2) between two SDRAMs.

3.8 External Memory Interface

NOR type and NAND type flash memories are employed for an external ROM interface to support up to two chips select signals and a 64Mbyte domain.

General I/O interface supports up to 4 chip select signals and a 16Mbyte domain for each select chip.

3.9 SATA/ATA Interface

3 channels for serial ATA interface are incorporated, which is the market standard. A 1.5Gbps serial ATA/1500 interface is supported to be capable of corresponding to HDDs with larger volumes and higher speeds. A channel for parallel ATA interface to support PIO mode and Ultra-DMA100 is also supported to be capable of corresponding to the HDD and optical drives.

3.10 Display Controller/BitBLT Engine

A powerful display controller engine is incorporated to enable ample video image quality to support the digital TV era.

The main display supports an HD-size video plane, three OSD planes and a background color. It is also capable of anti-flicker filter and alpha blending with the 256-color level.

The sub display supports an SD-size video plane and an OSD plane.

A color look up table of 2, 4 and 8 bpp, RGB32 and RGB16 modes is supported for OSD format so that various color formats are available.

The BitBLT engine supports a color space conversion function that is effective for high-speed block transmission of 2D images, motion adaptive IP conversion and various noise reduction functions.

3.11 External Video/Audio I/O

External input supports a digital video input based on ITU-R BT.656 and an audio input of PCM.

External output supports a digital video output compliant to ITU-R BT.1120/BT.655 formats for a digital output such as HDM. In addition, an audio output supports PCM data and an S/PDIF.

3.12 Video Encoder

Two output terminals, the main and sub video terminals are available. The main video output terminal can output YPbPr/YCbCr signals via a 148.5MHz/10-bit DAC. The sub video output terminal can output composite video output via a 54MHz/10bit DAC. A function to insert various signals into the vertical blanking interval is also supported.

3.13 Peripheral Functions

Most of the peripheral interfaces required for Hi-Vision DVD recorder are built in, such as a PCI bus with 33MHz/32bit compliant with PCI2.2 format, UART (3 channels), I2C (3 channels), smart card (1 channel), IR transmitter (1 channel), watchdog timer (1 channel) and general purpose ports, so that the numbers of LSIs in the system can be decreased.

4. Software Architecture

An example of the suggested standard software configuration for EMMA2RH is shown in **Fig. 2**. Available functions of each CPU are clearly divided. Also, by introducing communication drivers between CPUs, two types of OS, the RTOS and Linux can be employed in the architecture.

The RTOS is operated in the sub CPU to concentrate all functions including AV processing which requires real time processing by operating simultaneously with hardware.

The main CPU which provides high speed processing employs Linux. Linux is a general-purpose OS which supports the configuration of user applications. By employing Linux, a market standard OS, the development period has been reduced.

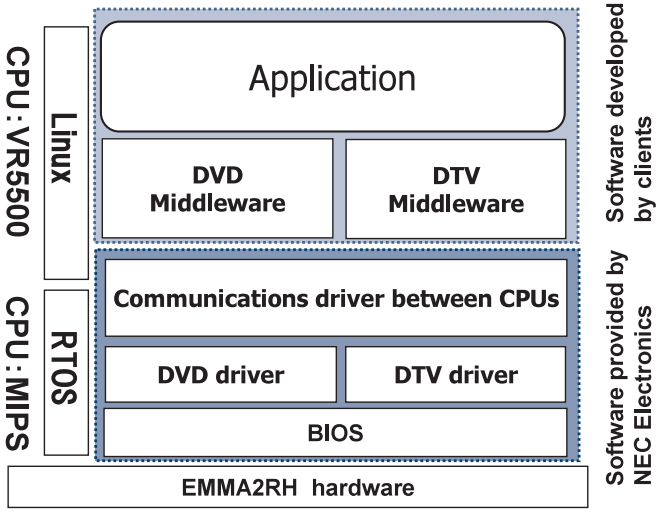

Fig. 2 EMMA2RH software configuration.

The software provided by NEC Electronics is software to be operated at a lower layer than the CPU communications driver, so that common interfaces may be incorporated that impose no direct influence on the hardware. These software interfaces may be used in common among EMMA families even for proposed future models.

5. Development Environment

An evaluation board of EMMA2RH is shown in **Photo**. This evaluation board mounts essential functions for a HDTV recorder to execute various evaluations with driver software provided by NEC Electronics. Moreover, this board is capable of Montavista Linux Professional Edition Ver.4.0. This will give an advantage to a software development environment for which applications to be operated on Linux can be booted at an early stage of the development.

6. Conclusion

This paper explains the features of the various functions of the EMMA2RH LSI chip. Employing this LSI enables the integration of DVD recorder systems for HDTV broadcasting into a single chip so that the high performance recording of two programs simultaneously and at low cost is enabled.

It is expected that the market for DVD recorders will continue to increase. NEC Electronics will provide various types of system LSIs for these DVD recorders and their application devices and will continue to develop and market more innovative products to support them.

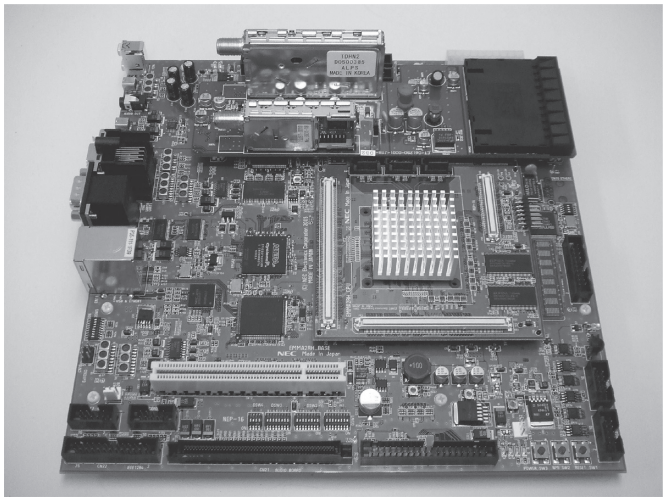

Photo EMMA2RH evaluation board.

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