

Technology for High Reliability System LSIs

MOCHIZUKI Yasunori, HAYASHI Yoshihiro, ODA Noriaki, TAKEUCHI Kiyoshi, TAKEDA Koichi

Abstract

The IT terminals and devices of the Ubiquitous age are required to be safe and robust as well as being highly convenient and there is also a need for a greater reliability of the system LSIs that they use. Moreover, in the case of the most advanced LSIs that are under continual performance improvement, the microminiaturization is approaching its physical limit so that the prevention of ageing and circuit malfunctions is becoming more important than ever. This paper introduces the recent developments in LSI reliability improvement technologies that have been developed by NEC for use in supercomputers and car-mount systems in which reliability over a wide temperature range is a critical feature.

Keywords

system LSI, supercomputer, car-mount, reliability, multi-layer wiring, SRAM, variance

1. Introduction

System LSIs may be embedded in many locations, in equipment that is very familiar to individuals such as PCs, cellular phone terminals and home appliances to systems supporting the foundations of the IT society such as broadband equipment, wireless communication infrastructures and supercomputers. It is no exaggeration to say that the LSI is one of the main actors in supporting the Ubiquitous society. The devices of the future Ubiquitous society are required to achieve both an “anytime, anywhere capability” and a “more advanced convenience.” In order to create an environment in which chips are ubiquitous throughout daily life, the LSIs themselves are required to achieve high standards of environmental resistance as well as a higher device reliability than at present. Meanwhile, the performance of system LSIs has progressed significantly as a result of the advancement in microminiaturization and the reliability improvement technologies will become more important than ever for continuing to improve performances in the future.

NEC has offered system LSIs for use in supercomputers in order to support the need for an extremely high performance as well as in car-mount systems that must feature reliability over a wide range of temperatures. In the present paper, by focusing on the fields of device and circuit technologies we will describe the core technologies that are proposed for improving the LSI reliability that will be an essential feature of the products of the next generation.

2. Highly Reliable Multi-Layer Wiring Technology

The material used for the multi-layer wiring of system LSIs has been changed from aluminum to copper, which is now used in the LSI products for use in the Earth Simulator (180nm generation). Now, the advanced LSI mass-products have entered the 90nm generation and their wiring size has halved compared to the 180nm generation. With the 65nm generation now under development and the 45nm generation being researched, microminiaturization will be advanced to respectively 35% and 25% that of the 180nm generation, and the number of wirings on the LSI will undergo a 10 fold increase, to number more than ten million wirings. The advancement of microminiaturization and the increase in scale have placed wiring reliability as one of the key items differentiating the LSI. Wiring reliability is regarded as being particularly critical for the ultra high-speed MPU that needs a high speed and a high current and the car-mount LSIs that are used under high environmental temperatures.

There are some modes in which the reliability of micro-wiring degrades. Electro-migration (EM) is a phenomenon with which the density of electrons flowing through the wiring increases due to microminiaturization and their collision with copper atoms produces voids, eventually leading to a wiring disconnection. Stress migration (SM) is another mode causing wiring disconnection due to stress. In addition, time-dependent dielectric breakdown (TDDB) is increasing due to the mechanical and electrical weakness of the low-permittivity interlayer insulation films that have recently been introduced to reduce the inter-wiring parasitic capacitance¹⁾.

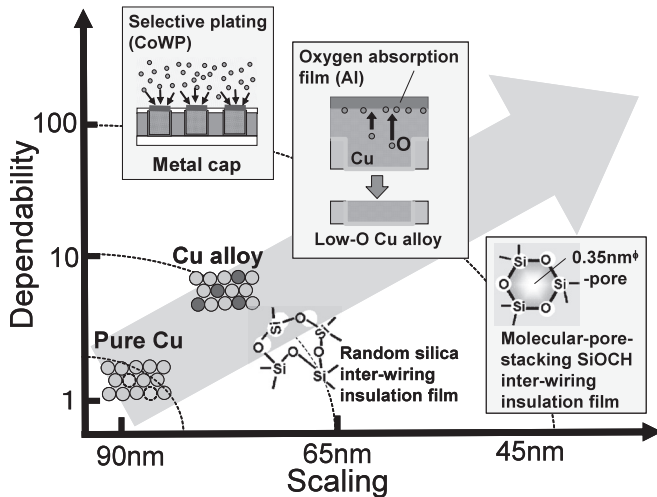


Fig. 1 Reliability improvement technology for the advanced LSI multi-layer wiring.

To deal with these reliability-related issues, we have been developing reliability improvements at the molecular and atomic levels based on the knowledge of materials physics and chemistry (Fig. 1). With the 65nm generation, we developed the Cu alloying technology, which adds impurities to copper wiring to restrict the diffusion of the copper atoms^{2,3}, and improve the EM/SM resistance by 5 to 10 times. In addition, we also developed technologies for the 45nm generation such as low-oxygen copper alloy wiring⁵ and molecular-pore-stacking film¹.

With the previous technology, a small amount of oxygen (O) in the copper (Cu) film was diffused during thermal treatment for alloying/crystallization and oxidized the metallic film (Ta/TaN) in the substrate barrier, thereby degrading the SM resistance of microvias. The low-oxygen copper alloy wiring technology prevents the occurrence of this phenomenon by forming an oxygen-absorbing film (sacrificial film) on the copper film in order to absorb oxygen from the copper film during the alloying/crystallization process. We also developed a new film material (molecular-pore-stacking SiOCH film) that has a mechanically stable hexagonal molecular skeleton to replace the previous organic silica (SiOCH) film that has an irregular structure. This material has succeeded in implementing a porous film featuring low permittivity and excellent moisture absorption resistance by controlling the diameters of the voids in the film at no more than 0.5nm . Fig. 2 is an electron micrograph of a multi-layer wiring module applying the reliability technologies above. It shows that the oxidation of Ta along the grain boundary of the barrier film metal is suppressed for the

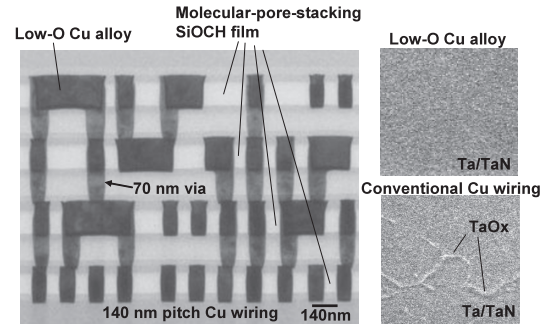


Fig. 2 45nm generation multi-layer wiring structure and reduced barrier film oxidation by low-oxygen Cu wiring.

low-oxygen copper alloy wiring.

We are also developing a metal cap technology for the improvement of wiring reliability⁶. It coats the copper wiring surface selectively with a WCoP thin film by means of a selective plating process in order to completely block the diffusion of copper atoms on the wiring surface. Although there are still some issues to be resolved such as a required improvement in the selectivity of the plating process, we have already confirmed improvement of the EM resistance by about a factor of 100^6 .

3. A New SRAM Microminutuarization Technology

The on-chip memory (SRAM) is one of the fundamental building blocks of system LSI. As a result of LSI performance improvement by microminutuarization of the CMOS process, it has now become difficult to assure compatibility of the data read margin (noise margin) and the write margin of the SRAM. With traditional SRAMs, a memory cell was composed of a combination of six transistors (6Tr-SRAM), but we have begun the development of a new memory technology that will be able to break down scaling limits and to thus pioneer the road to higher performance LSIs.

The technology that we have recently developed in order to prevent data destruction due to the degradation of noise margins consisted of creating an SRAM cell using seven transistors (7Tr-SRAM) by adding a data protection transistor to a 6Tr-SRAM cell as shown in Fig. 3. While the traditional 6Tr-SRAM design performance is troubled by the tradeoff between the operational stability and speed, the 7Tr-SRAM makes it possible to improve both the operational speed and noise margins.

The memory cell area of the 7Tr-SRAM is naturally in-

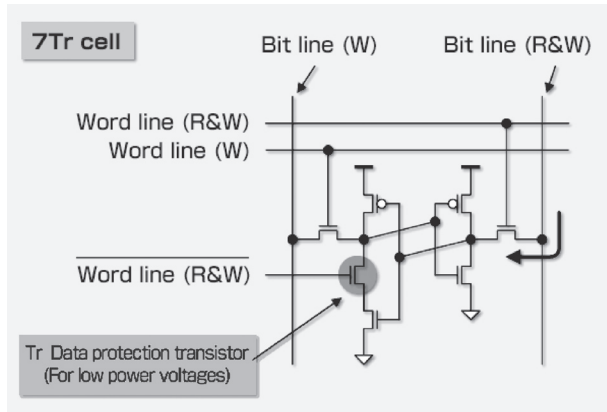


Fig. 3 7Tr-SRAM cell.

creased due to the addition of a transistor, but this increase is compensated by developing a new layout technology, in which a sense amp is embedded in the memory cell array. This design has succeeded in reducing the increase in the memory cell area to only 10% compared to the 6Tr cell area, while the increase would be 30% if this design was not adopted. When the micro-miniaturization is advanced even further in the future and if the 6Tr-SRAM is still used then, it is expected that the cell area would be increased even more than in the current trends in order to ensure the operational reliability. However, since the 7Tr-SRAM has excellent operation stability, there is a potential that it will no longer be disadvantageous in terms of the cell area and can be implemented with a smaller cell area than the 6Tr-SRAM of the same operation speed.

Fig. 4 shows a 64Kb SRAM that was prototyped using a 90nm CMOS. The currently most advanced, 90nm generation LSIs use a supply voltage of 1.0V, and the SRAM macro shown in this figure achieves an ultra high-speed, 1GHz operation using the same supply voltage. Furthermore, the recent solution of the SRAM margin issue has made stable operation possible even when the supply voltage is as low as 0.5V. In addition, another problem with the traditional 6Tr-SRAM is that the operation speed of the SRAM drops more suddenly than that of the logic circuitry when the supply voltage drops. However, with the 7Tr-SRAM, we have confirmed that it can maintain the same delay characteristics as the CMOS logic circuit even with a supply voltage of 0.5V.

As described above, the 7Tr-SRAM technology makes it possible to maintain the trends in both the speed increase and voltage reduction of SRAM and to scale the SRAM in the same way as the logic circuit even in the 45nm generation and after. This technology will lead to the implementation of an

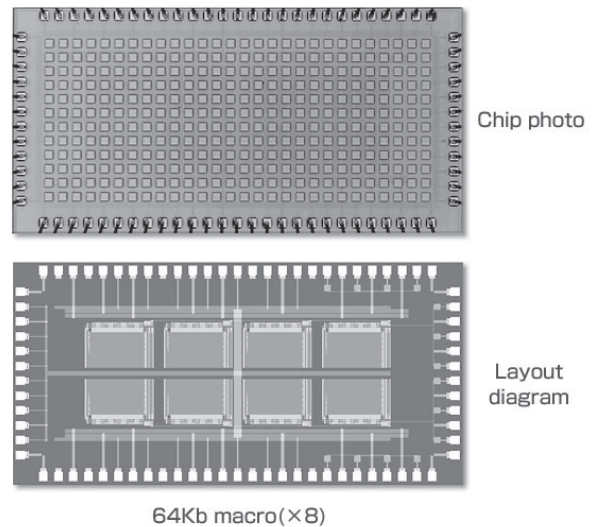


Fig. 4 90nm-CMOS 64kb-SRAM macro using 7Tr cells.

ultra high-speed consolidated memory that will be an essential component of the next-generation, GHz-class system LSIs and high-speed computer systems.

4. A Statistical Circuit Simulation Technology for Dealing with Variations

The microminiaturization of LSIs has led to an increase in variations in the device characteristics. Although the characteristics of devices used for LSIs should ideally be uniform, the circuitry for micro-devices of the 90nm generation and after should now be designed assuming a certain degree of disorderly change. The design should maintain headroom for absorbing such variations in order to assure stable operation of the circuitry under this constraint. However, an excessive increase in the headroom would tend to degrade the performance of the circuitry. Therefore, to design circuitry that features both high reliability and high performance, it is necessary to optimize the design in an advanced manner based on a detailed understanding of the variations of devices. Statistical circuit simulation is a feature of such an advanced design. Statistical circuit simulation adds, to the circuit simulation that has long been applied in circuit design, an ability to consider variations of device characteristics quantitatively.

Statistical circuit simulation needs a technology that can translate the variations in device characteristics into that of the

parameters used by the simulator (variation model determination). However, a method for performing such translation efficiently has previously been unattainable and this fact has been an obstacle to the practical implementation of statistical circuit simulation. This problem has been overcome by a new technique that we have developed.

With the previous technique, the variation model was determined by first determining the set of parameters representing the characteristics of each of the devices with varied characteristics by means of parameter fitting operations, and then checking the statistical properties of the parameter set determined above, as shown in the left flowchart of Fig. 5. However, with this technique, the complicated parameter fitting operations (in Fig. 5, this corresponds to the step in which the parameter set is extracted from the I-V characteristic) should be repeated for the same number of times as the number of devices (this sample size may be as high as some hundreds) and the obtained variation model is doubtful in both quality and reliability.

On the other hand, the newly developed technique determines the variation model directly from the statistical properties of the device characteristics (in Fig. 5, statistics of measured I-V) as shown in the right flowchart of Fig. 5. This technique does not need to repeat the complicated parameter extraction operations and can determine the variation model very quickly. In addition, it also presents other significant features, including the possibility of representing variations efficiently by using a smaller number of parameters and its applicability regardless of the simulator type.

The variation model determined using the new technique allows the simulator to reproduce the actual variations in device characteristics with high accuracy. Fig. 6 shows an example of

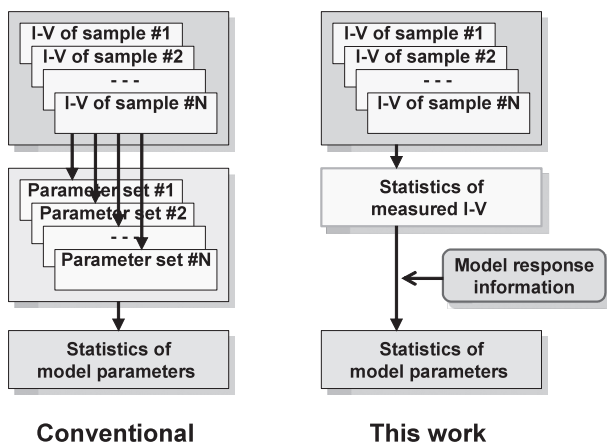


Fig. 5 Efficient determination of variation model.

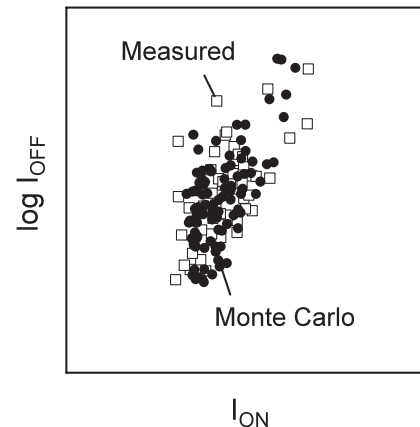


Fig. 6 Comparison between the simulation results using variation model and the actual measured results.

the application of this technique, in which the variations of the on and off currents of many transistors are reproduced accurately by simulations (dots indicated as Monte Carlo in Fig. 6). The newly developed statistical circuit simulation technology enables circuit design with an advanced statistical consideration and the implementation of high-speed, stable circuitry with logic CMOS-LSIs for the 90nm generation and after.

5. Conclusion

In the above, by focusing on the development results in the fields of device and circuit technologies, we described the advanced system LSI technologies for supporting reliability that will play such an important role in future supercomputers and car-mounted electronics.

System LSIs are products that vertically integrate the technologies of various layers from materials/device technology to circuits, architectures and software technologies. It is said that in order to advance LSI performance further and improve reliability, collaborative breakthroughs covering a wider range of technology layers than hitherto will be necessary. At NEC, we intend to accurately identify technological trends and to develop supporting system LSI technologies for the Ubiquitous age that will feature “advancement of services” and an “any-time, anywhere capability.”

References

- 1) Hayashi, Applied Physics, Vol. 74, No. 9, p.1178 (2005).
- 2) Matsubara, et al., Symp. VLSI Tech., Digs. p.127 (2003).
- 3) Tonegawa, et al., IEEE IITC 2003, Proc., p.216 (2003).
- 4) Abe, et al., IEEE Int. Electron. Device Mtg., p.83 (2005).
- 5) Ishigami, et al., IEEE IITC 2004, Proc., p.75 (2004).
- 6) Oda, et al., IEEE Int. Electron. Device Mtg., p.1045 (2005).
- 7) Takeda, et al., IEEE ISSCC 2005, Proc. p.478 (2005).
- 8) Takeuchi and Hane, Int. Conf. Simulation of Semicond. Processes and Devices (SISPAD), p.135 (2005).

Authors' Profiles

MOCHIZUKI Yasunori
Chief Manager, Research,
System Devices Research Laboratories,
NEC Corporation

HAYASHI Yoshihiro
Research Fellow,
System Devices Research Laboratories,
NEC Corporation

ODA Noriaki
Team Manager,
Advanced Device Development Division,
NEC Electronics Corporation

TAKEUCHI Kiyoshi
Principal Researcher,
System Devices Research Laboratories,
NEC Corporation

TAKEDA Koichi
Assistant Manager,
System Devices Research Laboratories,
NEC Corporation