System LSI Development Is Changing!

R&D of the high-level design automation system "CyberWorkBench"

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We are sometimes astonished by the recent advances in cellular phones and digital home appliances that feature a wide range of new capabilities. These advances are supported by the system LSI technology, which integrates a large number of functions on a single chip. However, as the advances have also increased the burden on the field of development, design technologies that enable quick and efficient development are urgently required at the present time.

The technology regarded as the mainstream one among the new design technologies is "C-based design," that employs C-language, which is an established language in the field of software for enabling circuit design by simply describing its behavior. We here report an interview with Dr. Kazutoshi Wakabayashi at the NEC System Devices Research Laboratories, who is an international authority on this technology, who is also the developer of the high-level design automation system "CyberWorkBench."

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The final bottleneck in system LSI design automation lies in the high-level design process

Since its start in the 1960's, the history of system LSI design automation or CAD (Computer Aided Design) has been advancing from the back-end process toward higher level. Namely, automation was begun with the masking and packaging layout process before the production process and that the gate-level schematic generation based on logic design followed them.

"It was only in these ten years or so that automation of the more intellectual design processes in higher level has begun to advance. Since the 1980's, we have started to use a logic synthesis tool to generate logic-level circuitry from RTL (Register Transfer Level) descriptions in the process for automatic schematic generation from the logic design, and this tool employs a special language such as Verilog-HDL (HDL: Hardware Description Language) or VHDL," explained Dr. Wakabayashi.

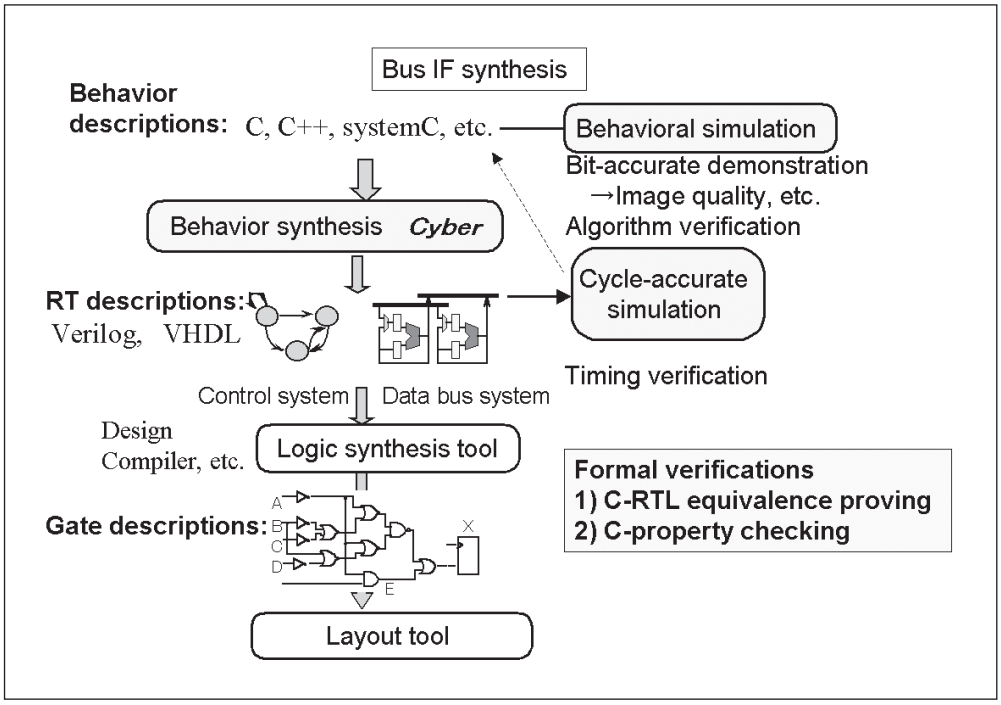

Fig. 1 LSI design process incorporating "C-based Design."

"The present issue is to develop a tool for automating the stages from the high-level system design to the behavior description and linking them to the RTL and later processes. This tool is called the "behavior synthesis tool" or "high-level synthesis tool" in specialist terms. A similar "behavior synthesis tool" has already been marketed a few years ago for VHDL and Verilog. However, it was not widely adopted due to the large number of restrictions in describing behavior, the low quality of the synthesized circuitry and the low usability caused by insufficiency of functions. Our aim was to build a design environment in which 'C-language,' the standard program language in the world of software technology, can be used, and to enable the automatic conversion of a behavior-describing program into RTL. We were told in the beginning that it was impossible, but it has subsequently become an important worldwide trend of 'C-based design'."

Figure 1 shows the LSI design process incorporating the "C-based design." The "behavior synthesis tool" developed by Dr. Wakabayashi et al. is named the "CyberWorkBench."

Design scale reduction is not the only benefit

"CyberWorkBench" is a very powerful tool. For the result of a calculation made based on actual examples of development of MPEG decoder chip, etc., "the code size is only 1/7 of RTL and 1/28 of the gate level, and the simulation time is as short as several tens or hundreds of that of RTL. We actually spent only 6 hours in completing a chip that may usually take a week to complete." It is easy to understand that code size reduction improve design process efficiency; it is because the C-language is a high-level language and features a higher degree of abstraction. Design period can be reduced by more than 50%. It can facilitate corrections in debugging, increase the simulation speed and also presents other advantages including improvements in the reliability of chips. In addition, its power is also noticeable from the aspect of its design "quality".

"In design, it is not unusual that trade-off occurs between the chip area, processing performance, and other factors. A larger chip can increase the processing speed and a reduced chip area will decrease the speed, and so on. The

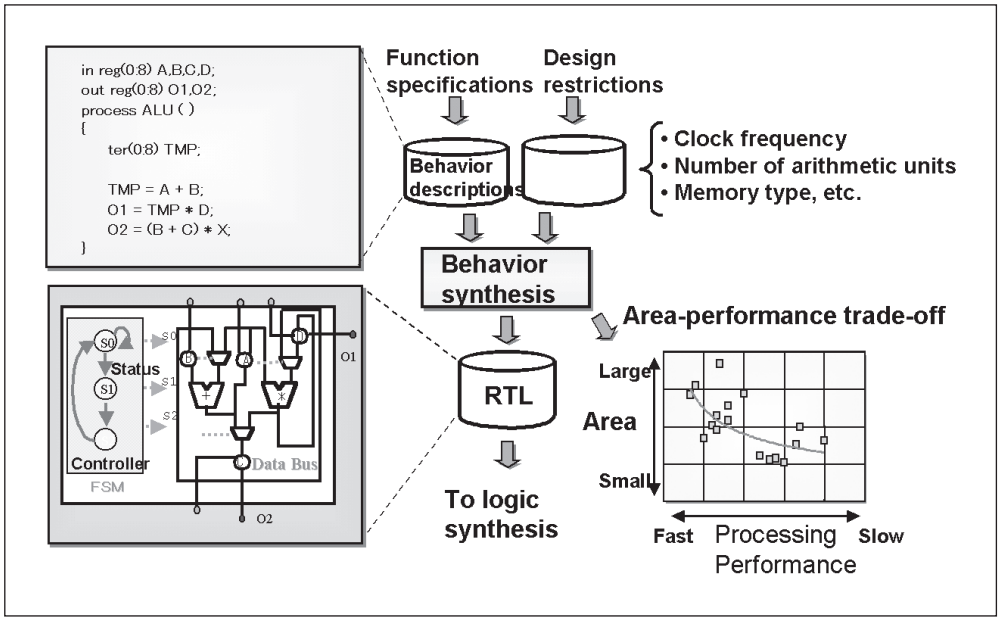

Fig. 2 Behavior synthesis.

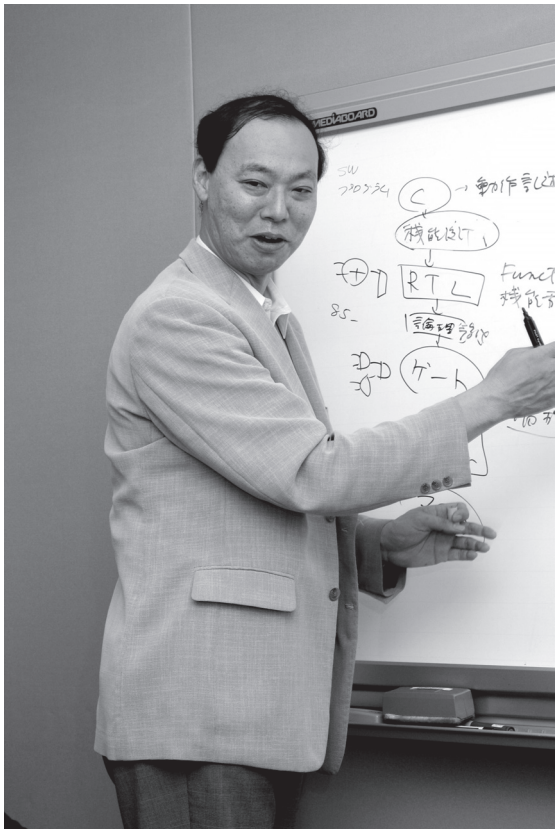

Photo 1 Dr. Wakabayashi explaining his research field.

designer needs to select appropriate design by considering such antagonisms, but the logic synthesis of RTL allows only small varieties of design and the options are limited. However, the behavior synthesis tool can generate several patterns with several kinds of variables for the components (**Fig. 2**). This will lead to a greater difference when the case of developing several kinds of chips for the same application. With RTL, every kind of chip has to be developed individually, while the behavior synthesis tool can do all at once. When we developed three kinds of encryption/decription chip, we could actually reuse only one set of behavior description data. It is not at all an exaggeration to say that the behavior synthesis tool "CyberWorkBench" has a power capable of radically innovating techniques for the development of LSI systems."

A highly perfected tool equipped with a verification capability was created

"CyberWorkBench" is not used exclusively for behavior synthesis. It also integrates the verification function that is critical in chip development. This function enables program debugging and guarantees that the behavior synthesis described in "C" and the result of conversion into RTL are equivalent.

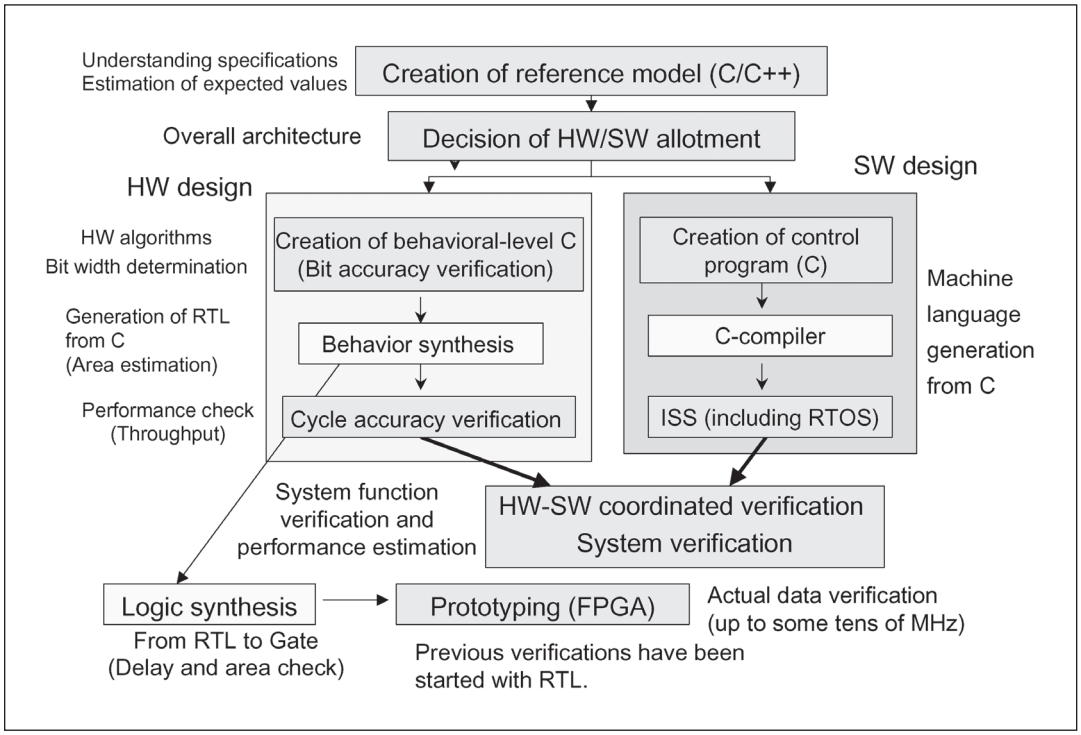

Fig. 3 LSI design procedure of C-based design.

"CyberWorkBench" generates a simulation model in addition to the RTL hardware design data. A separately developed hardware-software coordination simulator enables verification of a chip and also embedded software. Furthermore, faster verification is also possible by running the obtained RTL design data on a reprogrammable logic device, FPGA (Field Programmable Gate Array). This makes it possible to confirm that simulated behavior can be executed without an error from the originally intended operations of the system LSI (**Fig. 3**).

You might ask how this tool that offers an environment with such a high degree of perfection was developed.

"It took time. We started to work on it eighteen years ago, when logic synthesis (automation of logic descriptions), which is a far cry from behavior synthesis, had just begun to be used in the field of LSI for general-purpose machines. We applied the behavior synthesis technique in controller design for a transmitter-dedicated processor and achieved a favorable result. Later, we repeated similar trials every whenever we had an opportunity, and eventually succeeded in creating the first commercial-purpose chip using the "C-based design" technique in '94. Our environment did not feature a verification function at that time. It was since around '99 that an increased number of other in-house departments began to express their will to use it. We get trusted through the real chip experience and, particularly after the success in a project for developing new large-scale circuitry for cellular phones in a short period, the "C-based design" came to be accepted rapidly at NEC."

Figure 4 shows some of the actual achievements of Dr. Wakabayashi et al. It shows how wide the application of this technology actually is.

"C- based design" is inseparable from the paradigm shift in design techniques

Dr. Wakabayashi says, "Perhaps NEC is the only company that can handle the "C-based design" so well at the commercialized chip level." The biggest factor making this possible was the fact that "enabled design in C language" as it was intended from the beginning, but he also pointed out two other prominent factors.

"From the beginning, CAD tools have been

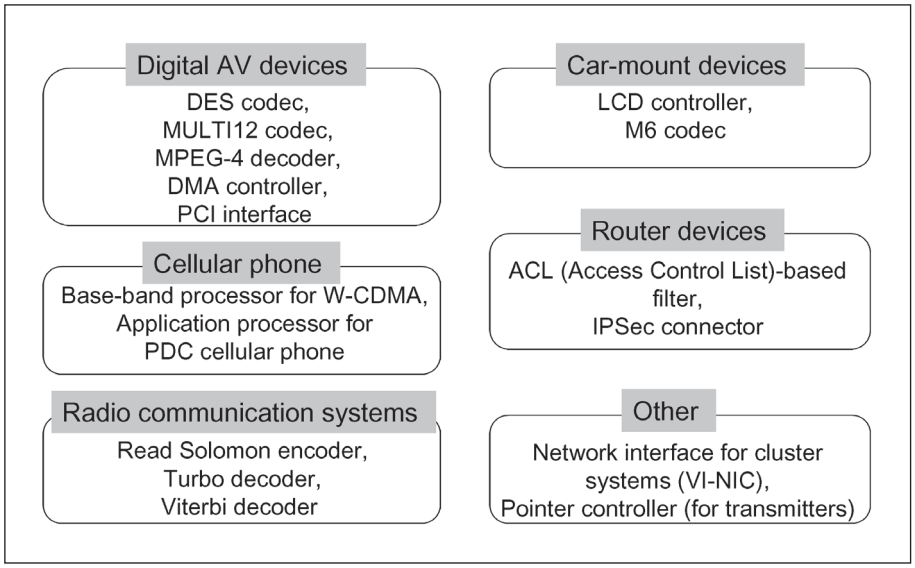

Fig. 4 Achievements of "C-based design."

polished and advanced in the process of the in-house production of chips. However, the majority of manufacturers outsource these kinds of chips, recently. This practice usually prevents the design and manufacturing departments from developing inter-departmental idea. However, the NEC Group has succeeded in maintaining an environment that encourages improvements based on in-house cooperation. This was another factor. And the last factor is that we did not attempt to create a perfect tool from the beginning. Instead, we took more realistic approach of improving the functionality step by step in order to prepare and arrange an optimum environment gradually."

In spite of his words, Dr. Wakabayashi does not seem to be completely optimistic about the present status of the "C-based design."

"Many designers still say that the traditional RTL or, writing with assemblers if I use the terms of software programming, is more convenient because it is more flexible. This is certainly not wrong if we consider the cases of the fine adjustment of a circuit or a minor improvement of a function. However, from the macroscopic viewpoint of rationality, there is no countermeasure to be taken against the problem of a continuous increase in the design scale. I wish that designers would consider the fact that system LSI has now entered a new stage where a paradigm shift from the existing design techniques is necessary.

Traditional circuit design is 'to think in terms of structure,' and the C-based design is 'to think in terms of behavior.' We should think in terms of algorithms and behavioral sequences rather than of components such as registers and arithmetical computing units. This is a 'paradigm shift.' Design engineers sometimes have difficulty in understanding it and I find that software engineers like those who handle embedded equipment usually understand it more easily."

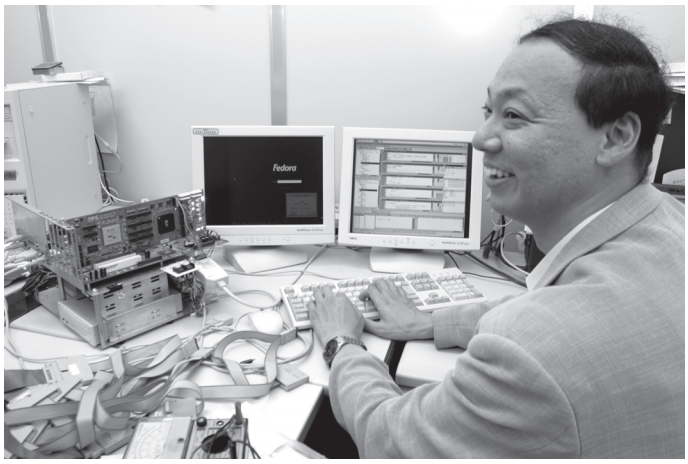

Photo 2 System development scene.

The award of honors is only a step in the challenge of "transforming the computers"

Dr. Wakabayashi is working very hard in academic society by contributing many papers and presentations to international CAD conferences and always appeals for the need for a "design paradigm shift." He can be compared to an evangelist for "C-based design." Recently, these activities were approved in the form of the FY2004 (4th) Yamazaki-Teiichi Prize by the Foundation for the Promotion of Material Science and Technology of Japan. With this award the foundation appreciates the contribution by Dr. Wakabayashi of "An exceptional Japan-originated system LSI design technology that Japan can really be proud of and which can be evaluated highly from every point of view, including its originality, technical standard, industrial impact and future potential."

But the award of this honor does not seem at all to give a rest to the R&D challenges of Dr. Wakabayashi. One of his latest challenges, the development of the DRP (Dynamically Reconfigurable Processor) compiler is an extension of the results achieved in the development of the behavior synthesis tool using the "C-based design" and in projects applying it. Simply speaking, the DRP is an LSI capable of organizing its own circuitry as required according to the program, and which is equipped with a parallel processing capability and a large memory function. It is said to be suitable for packet and stream data processing in the communication field, but Dr. Wakabayashi sees much more potential in it.

"When the DRP becomes widely available, it will be able to replace general-purpose microprocessors and DSP (Digital Signal Processor) chips and programmable chips with a high performance and low power will be the mainstream. I have long wished to offer a challenge by attempting to transform the future of computers, and I believe that this would be the first step on this path."

The words added by Dr. Wakabayashi at the end of the interview suggest another aspect of his personality that is far removed from simply being ambitious:

"I feel a debt of gratitude toward the successive top management of our house, for they have always watched over our research, even before it had become clear that our work would amount to something. I should like to repay their favors by assisting other LSI engineers and making a contribution thus to the revival of the device industry in Japan."

(Interviewed/compiled by Haruhito Tsuchiya)